TP 10.5: A 13.4-GHz CMOS Frequency Divider

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The potential of deep submicron CMOS technologies for high-speed applications has been demonstrated in a number of circuits [1, 2]. The density, low-voltage operation, and low power of CMOS devices make them attractive for compact integration of communication systems.

This paper describes the design of a 13.4GHz 1/2-frequency divider fabricated in a partially-scaled 0.1μm bulk CMOS technology [3]. The circuit design is heavily influenced by the device structures and layout rules.

To reduce both fabrication cost and turnaround time, the CMOS process scales only channel length to 0.1μm and gate oxide to 40Å [3]. Design rules for other dimensions correspond to a 1μm technology, yielding a minimum source/drain area of 2.2x2.2μm². Thus the contribution of the source/drain junction capacitance is substantial, severely limiting speed.

The above difficulty is alleviated by use of ring-shaped transistors, where the ratio of device width and drain junction capacitance is approximately four times that of a regular layout [4]. However, such a structure proves beneficial if only one of the drain or source terminals appears in the signal path. Thus, high-speed divider topologies using stacked devices or pass gates do not necessarily achieve a higher speed if they incorporate this structure. Another drawback of typical divider topologies stems from their use of pMOS devices in the critical signal path. The transconductance-input capacitance trade-off of these transistors degrades speed significantly.

The divider described employs the following techniques to improve the speed: 1) nMOSFETs for sensing and regeneration and pMOSFETs for pull-up, 2) no stacked devices and pass gates, 3) ring-shaped geometry for all transistors. As a result, it both lends itself to partially-scaled technology and achieves a maximum speed relatively independent of pMOS characteristics. The divider block diagram is shown in Figure 1. The circuit employs two D-latches in a master-slave configuration with negative feedback. While in high-speed master-slave dividers it is common practice to design the slave as the "dual" of the master so that they can be both driven by a single-phase clock, the divider of Figure 1 uses two identical latches driven by CK and $\overline{CK}$. In order to minimize the skew between CK and $\overline{CK}$ the non-inverted phase is delayed by a complementary pass gate [4]. Simulations show skew between CK and $\overline{CK}$ in this circuit is <10ps for a 13GHz sinusoidal input.

Figure 2 depicts the divider circuit. Each latch consists of two sense devices (M_1 and M_2 in the master and M_7 and M_8 in the slave), a regenerative loop (M_3 and M_4 in the master and M_9 and M_{10} in the slave), and two pull-up devices (M_5 and M_6 in the master and M_{11} and M_{12} in the slave). When CK is high, the master is in the sense mode while the slave is in the store mode, and when CK goes low, the reverse occurs. Since the gate-source capacitance of the pMOS transistors does not appear in the critical path, the transcoductance-input capacitance trade-off of these devices has little effect on divider speed.

In contrast to conventional latch topologies, the D-latch circuit used in this divider does *not* disable its input devices when it goes from the sense mode to the store mode, thus avoiding stacked transistors. While this poses timing problems in a general digital circuit, it does not prevent the divider from functioning properly. Two observations explain this. First, since the input devices of each latch are n-type, they can change the state only if one of the inputs goes from low to high and the other from high to low. Second, when each latch is in the sense mode, neither of its outputs can go from low to high because the pMOS pull-up devices are off. Thus, if, for example, the master is in the sense mode and the slave in store mode, the master outputs can only go from high to low and hence cannot override the state stored in the slave.

Simulations based on CMOS device models are used to compare performance of the proposed topology with high-speed dividers reported in [1] and [5]. Plotted in Figure 3 is the maximum clock frequency of each circuit, f_{max}, as a function of supply voltage, indicating at least a factor of two improvement in speed.

The divider is fabricated in 0.1μm CMOS technology. Figure 4 is a micrograph of the die, whose active area is approximately 50x70μm². The circuit is tested on-wafer at room temperature using a high-speed Picoprobe to apply the input and a Cascade multi-contact probe to measure the output as well as provide power and ground connections.

Shown in Figure 5 are measured divider input and output waveforms at f_{CK}=13.4GHz with 2.6V supply. Input amplitude is rail-to-rail. No attempt is made to generate large output swings off-chip, as the setup provides sufficiently high signal-to-noise ratio, allowing direct measurement of amplitudes in the millivolt range. The output stage of the circuit is simply a 3μm/0.1μm nMOS transistor driving a 50Ω load.

To assess low-voltage performance, the supply voltage is varied from 1.2 to 2.6V, yielding the f_{max} variation in Figure 6. The divider has an f_{max} of 5GHz at V_{DD}=1.2V and 10GHz at V_{DD}=2V. In comparison, the 0.1μm SOI implementation in [1] has f_{max} of 2.6GHz at V_{DD}=2V.

The measured speed-power trade-off of the prototype (including I/O buffers) is shown in Figure 7. The circuit dissipates 2.6mW at 5GHz (with V_{DD}=1.2V) and 28mW at 13.6GHz (with V_{DD}=2.6 V). Since the primary goal is high speed, all devices are ring-shaped and hence have a minimum width of 10μm. For clock frequencies below 10GHz, a design employing smaller devices reduces power by approximately 5 times.

References

[1] Fujishima, M., et al., "Low-power 1/2 Frequency Dividers Using 0.1μm CMOS Circuits Built with Ultrathin SIMOX Substrates," IEEE J. Solid-State Circuits, vol. 28, pp. 510-512, April 1993.

[2] Kado, Y., et al, "A 1-GHz / 0.9μW CMOS/SIMOX Divide-by-128/129 Dual Modulus Prescaler Using a Divide-by-2/3 Synchronous Counter," IEEE J. Solid-State Circuits, vol. 28, pp. 513-517, Apr. 1993.

[3] Lee, K. F., et al., "Room Temperature 0.1μm CMOS Technology with 11.8 psec Gate Delay," IEEE IEDM, Dec. 1993.

[4] Weste, N., K. Eshraghian, *Principles of CMOS VLSI Design*, Addison-Wesley, MA, 1985.

[5] Yuan, J., C. Svensson, "High-Speed CMOS Circuit Technique," IEEE J. Solid-State Circuits, vol. 24, pp. 62-70, Feb., 1989.

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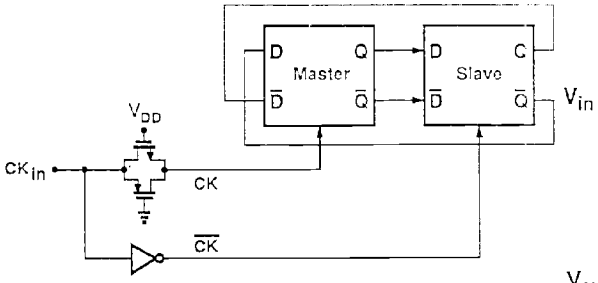

Figure 1: Divider block diagram.

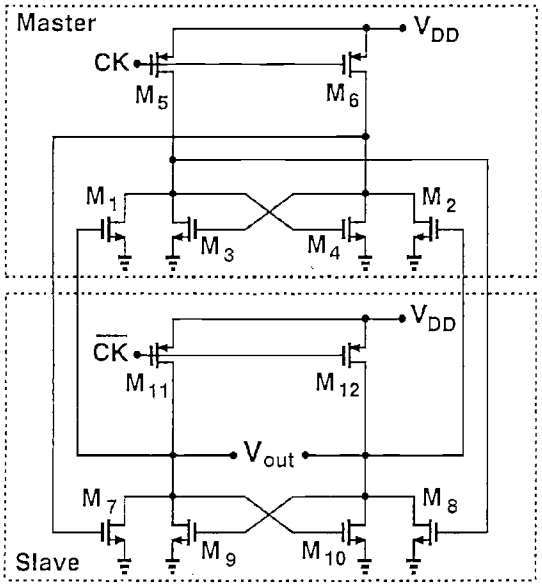

Figure 2: Divider circuit.

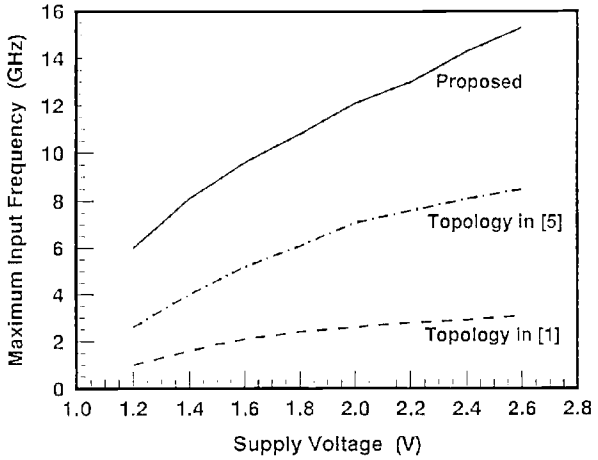

Figure 3: Simulated speed of divider and topologies in [1] and [5].

Figure 4: See page 333.

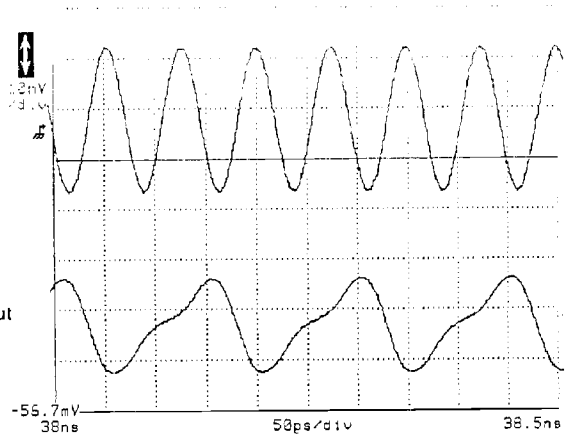

Figure 5: Measured input/output waveforms at 13.4GHz (input amplitude not to scale).

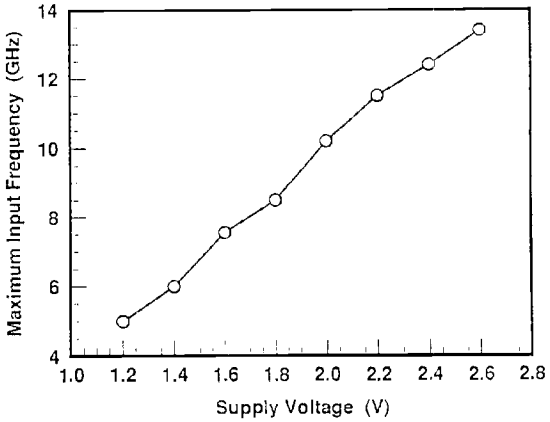

Figure 6: Measured speed vs supply voltage.

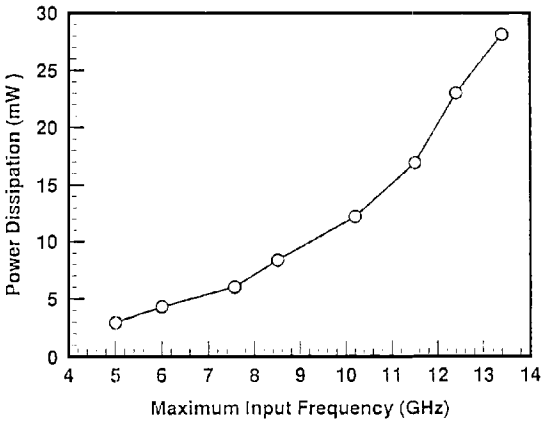

Figure 7: Measured power-speed trade-off.

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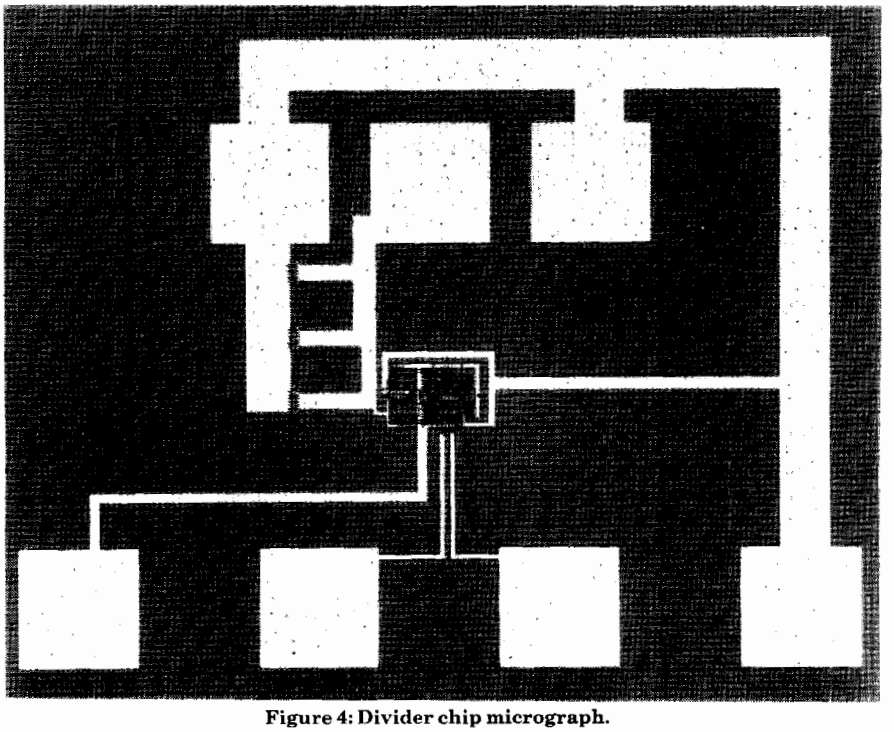

Figure 4: Divider chip micrograph.

TP 10.6: A 17dB Gain, 0.1 - 70GHz InP HEMT Amplifier IC

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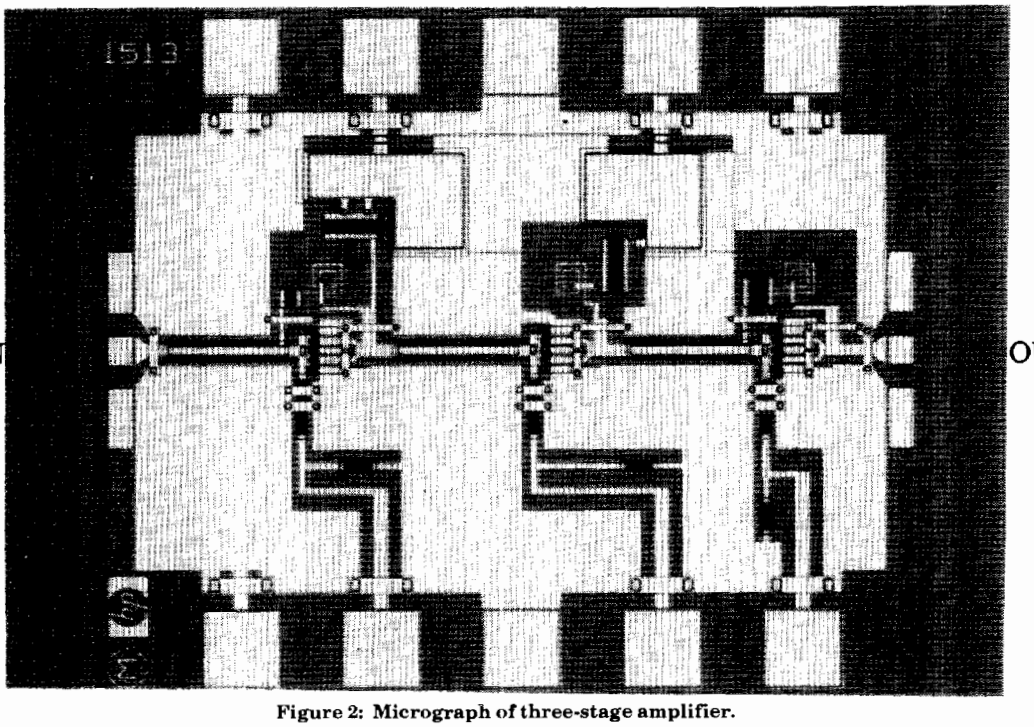

Figure 2: Micrograph of three-stage amplifier.