The Role of Monolithic Transmission Lines in High-Speed Integrated Circuits

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Abstract

This paper describes the role of transmission lines amenable to integration in VLSI technologies and their important circuit implications. First, an overview of microstrips, coplanar lines, and striplines is given and their performance limitations are quantified. Next, modeling and simulation issues are addressed and the role of transmission lines as circuit elements is discussed. Finally, examples of circuits that benefit from monolithic transmission lines are presented.

I. Introduction

Recent advances in high-speed circuits have heightened the interest in monolithic transmission lines (T lines)—as both parasitic components and useful devices. With the operating frequencies rising to several tens of gigahertz and/or the chip dimensions approaching several centimeters, T lines can degrade or enhance the performance of analog and digital circuits. Accurate modeling of T lines therefore proves essential in analysis and design. Furthermore, the additions of T lines to the device library allows designers to invent new circuit techniques, possibly transforming a parasitic to a useful component.

This paper deals with the impact of transmission lines on high-speed circuit design, focusing on their desirable roles in signal processing functions. Section II reviews T line structures suited to monolithic integration and their performance limitations in typical VLSI technologies. Section III presents modeling and simulation issues and Section IV summarizes useful attributes of T lines as circuit elements. Section V provides examples of T line circuit applications.

II. Monolithic T Line Structures

In order to identify T lines that lend themselves to fabrication in VLSI technologies, we first review the back end of a typical CMOS process. As depicted in Fig. 1 for a 0.13-μm generation, the process provides a silicided polysilicon layer and eight metal layers. Due to its high resistivity (about 5 to 10 $\Omega/\square$), the polysilicon layer is ill-suited to T line fabrication. Each of the first seven metal layers has a thickness of about 0.3 μm and a sheet resistance, $R_\square$, of 70 m$\Omega/\square$. The top layer typically has a thickness of 0.8 μm and $R_\square = 25$ m$\Omega/\square$. The metals are separated by two types of dielectrics: a 0.7-μm layer with $\epsilon_r \approx 3.5$ and a 0.1-μm layer with $\epsilon_r \approx 7$.

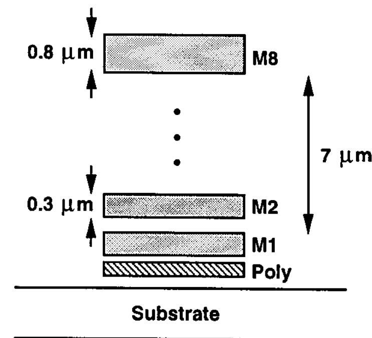

Fig. 1. Backend of a typical CMOS process.

The above back end example suggests three T line structures as candidates for monolithic integration. Illustrated in Fig. 2(a), the first is the microstrip topology, where a signal strip lies on top of a ground plane. As explained later, it is desirable to minimize the capacitance per unit length of the line, C_u, hence the use of M8 and M1 for signal and ground, respectively. Shown in Fig. 2(b), the second structure, a coplanar T line, employs widely-spaced signal and ground strips in M8 so as to reduce C_u. However, the signal line still exhibits substantial capacitance to the substrate.

Depicted in Fig. 2(c), the third structure is the stripline configuration, where the signal line is realized in an intermediate metal layer and it is shielded by ground planes in M1 and M8. Stacked vias provide vertical walls, connecting the two ground planes while confining the fields within the shield.

In circuit design, several properties of T lines become critical: characteristic impedance, loss, wave velocity, and field confinement.

A. Characteristic Impedance

For a lossless T line, the characteristic impedance, Z_0, is given by $Z_0 = \sqrt{L_u/C_u}$, where L_u and C_u denote the inductance and capacitance per unit length, respectively. As explained in Section V, most circuit applications of T lines require that C_u be minimized so as to accommodate larger transistor capacitances while still achieving a high value for Z_0. From this viewpoint, the microstrip and coplanar structures of Fig. 2 are advantageous over the stripline. For most T lines, the exact value of Z_0 must be obtained through the

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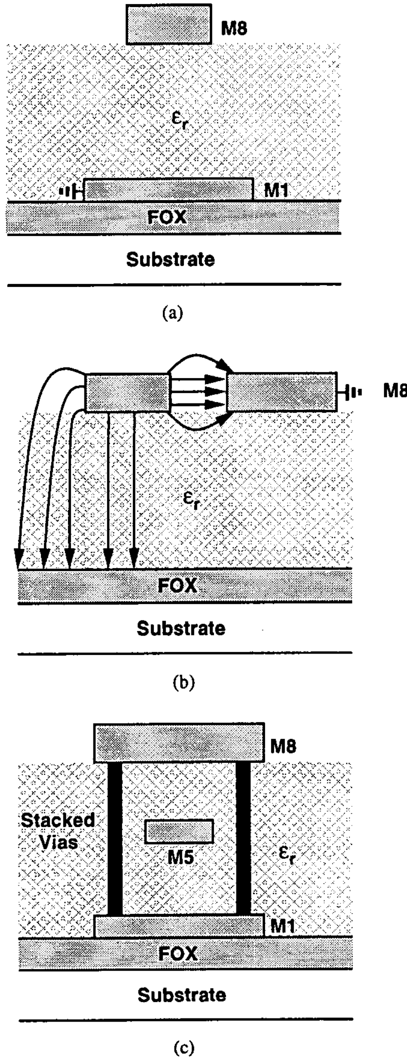

Fig. 2. Monolithic T line geometries, (a) microstrip, (b) coplanar line, and (c) stripline.

use of electromagnetic field simulators, but to develop intuition, closed-form expressions prove useful. In particular, for the microstrip geometry shown in Fig. 3, the characteristic impedance is given by [1]:

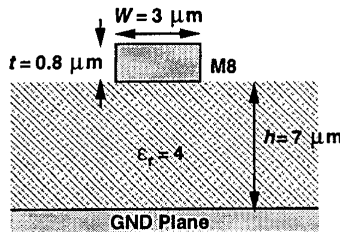

Fig. 3. Example of a microstrip dimensions.

$$Z_0 = \frac{377}{\sqrt{\epsilon_r}} \frac{h}{W_e} \frac{1}{1 + 1.735\epsilon_r^{-0.0724}(\frac{W_e}{h})^{-0.836}}, \qquad (1)$$

where

$$W_e = W + \frac{t}{\pi}(1 + \ln\frac{2h}{t}). \qquad (2)$$

In the back-end example of Fig. 1, $h \approx 7$ μm, $t \approx 0.8$ μm, and $\epsilon_r \approx 4$. If $W = 3$ μm, then $W_e = 3.98$ μm and $Z_0 \approx 94.3\,\Omega$. For $W = 4$ μm, Z_0 falls to 85.9 Ω.

B. Loss

The loss of microstrips arises from three sources: low-frequency resistance of interconnects, skin effect in interconnects, and dielectric loss[1]. The loss due to skin effect in the microstrip of Fig. 3 is expressed as [2]:

$$\alpha_{skin} = \frac{4.34}{\pi} \frac{R_s}{hZ_0} \left[1 - \left(\frac{W'}{4h}\right)^2\right] \times$$
$$\left\{1 + \frac{h}{W'} + \frac{h}{\pi W'}\left[\ln\left(\frac{2h}{t} + 1\right) - \frac{1 + t/h}{1 + t/(2h)}\right]\right\} \qquad (3)$$

for $2 \geq W/h \geq 1/(2\pi)$. In this equation,

$$W' = W + \frac{t}{\pi}\ln\left(1 + \frac{2h}{t}\right), \qquad (4)$$

R_s denotes the sheet resistance due to skin effect:

$$R_s = \sqrt{\pi f \mu_0 \rho}, \qquad (5)$$

and α_{skin} is expressed in dB/cm. For aluminum interconnects and $W = 3$ μm,

$$\alpha_{skin} = 2.156 \times 10^{-5}\sqrt{f}\ \text{dB/cm}. \qquad (6)$$

For example, at $f = 40$ GHz, $\alpha_{skin} = 0.431$ dB/mm.

It is instructive to compare the skin loss of a microstrip at $f = 40$ GHz with that due to its low-frequency resistance. This is accomplished by obtaining an equivalent resistance per unit length, R_{skin}, due to skin effect. The voltage wave at point x along a line is expressed as

$$V(x) = e^{-\alpha x}e^{-j\beta x}, \qquad (7)$$

where α denotes the loss and $\beta = 2\pi/\lambda$. The value of α_{skin} given by (3) is related to α as

$$\alpha_{skin} = -20\log(e^{-\alpha x}). \qquad (8)$$

Thus, $\alpha = 0.0496\ \text{mm}^{-1}$. For a T line with negligible dielectric loss,

$$\alpha \approx \frac{R_{skin}}{2Z_0}, \qquad (9)$$

which, for $Z_0 = 94.3\,\Omega$, yields $R_{skin} = 9.35$ Ω/mm. On the other hand, the low-frequency resistance of the metal 8 wire

[1] If the skin depth in the ground plane is greater than the metal thickness, the substrate may introduce additional loss.

is given by (25 m$\Omega/\square$) $\times$ (1000 μm/3 μm) $\approx$ 8.33 Ω/mm. The apparent resistance of the line therefore increases by about 12% as the frequency goes from zero to 40 GHz.

In addition to the above loss mechanisms, coplanar lines suffer from loss through the substrate as well [3]. Resulting from the electric field lines that terminate on the substrate (Fig. 4), this loss is much more significant in silicon technologies than in III-V processes.

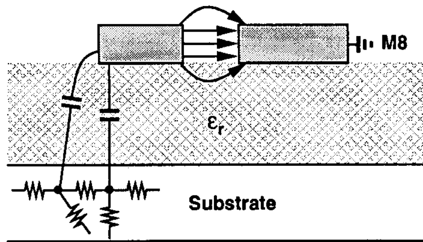

Fig. 4. Substrate loss in a coplanar line.

The trade-off between the characteristic impedance and the loss limits the performance of circuits using T lines. The resistivity of interconnects in standard silicon processes further exacerbates this issue.

C. Wave Velocity

The propagation velocity, v, in T lines determines the end-to-end delay that a signal experiences, playing a critical role in distributed oscillators (Section V). For a lossless line,

$$v = \frac{1}{\sqrt{L_u C_u}}. \quad (10)$$

An empirical expression for v in microstrips appears as [1]:

$$v = \frac{3 \times 10^8}{\sqrt{1 + 0.6(\epsilon_r - 1)(\frac{W_e}{h})^{0.0297}}} \text{ if } \frac{W}{h} < 0.6$$
$$= \frac{3 \times 10^8}{\sqrt{1 + 0.63(\epsilon_r - 1)(\frac{W_e}{h})^{0.1255}}} \text{ if } \frac{W}{h} > 0.6,$$

where W_e is given by (2). For the above example with $W = 3$, $v = 1.803 \times 10^8$ m/s and hence $L_u = 523$ pH/mm and $C_u = 58.8$ fF/mm.

D. Field Confinement

The leakage of fields from a T line to its environment can increase the loss whereas the leakage in the opposite direction can lead to noise coupling. In the coplanar geometry of Fig. 4, for example, noise in the substrate couples through the capacitances to the signal line. In this respect, the microstrip and particularly the stripline exhibit a higher performance. It therefore appears that the microstrip provides a reasonable compromise among Z_0, loss, and field confinement.

III. Modeling and Simulation Issues

As exemplified by the expressions in Section II, various empirical equations have been derived to predict the performance parameters of T lines. However, practical situations entail many complexities that require field simulators or even measurements to obtain the line parameters accurately.

Figure 5 illustrates a typical configuration in CMOS technology, where two metal 8 lines carry differential signals and the environment is filled with various dielectrics of different thicknesses. Furthermore, the ground plane has a finite width, W_G. The fringe capacitance between the signal lines lowers the characteristic impedance, while the heterogeneous dielectrics, the finite W_G, and the existence of the conducting substrate beyond the ground plane complicate the calculation of the line parameters. The key point here is that circuits such as distributed oscillators require a very small error (< 1%) in these calculations, making it difficult to neglect the second-order effects. Unfortunately, some common geometries cannot be handled even by today's field simulators, possibly mandating silicon iterations.

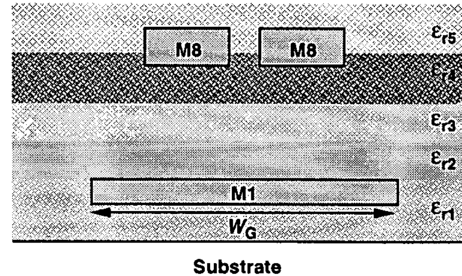

Fig. 5. Practical microstrip configuration.

While the inductance and capacitance per unit length can be obtained from Z_0 and v, it is sometimes simpler to compute them from Z or Y parameters. Field simulators typically treat a T line as a two-port network. As shown in Fig. 6, Y_{21} of a very short piece of the line can be used to directly determine the inductance per unit length:

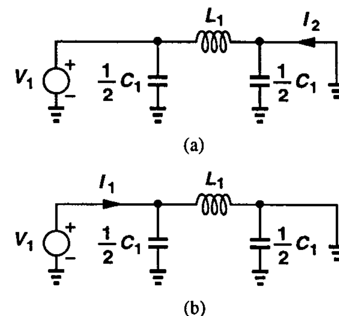

Fig. 6. Extraction of (a) inductance and (b) capacitance from Y parameters.

$$Y_{21} = \frac{I_2}{V_1}|_{V2=0} \quad (11)$$
$$= \frac{-1}{jL_1\omega}. \quad (12)$$

The capacitance of the line can also be obtained as depicted in

Fig. 6(b):

$$Y_{11} = \frac{I_1}{V_1}|_{V2=0} \quad (13)$$

$$= j\frac{1}{2}C_1\omega + \frac{1}{jL_1\omega}, \quad (14)$$

and hence

$$j\frac{1}{2}C_1\omega = Y_{11} + Y_{21}. \quad (15)$$

With the inductance and capacitance values known, Z_0 can be calculated and compared with that provided by the program to ensure proper simulation.

Circuit simulation programs typically provide T line models that are uniquely defined by Z_0, loss, and v, thereby allowing a mixture of T lines and other devices in a circuit. However, in some cases, it is more intuitive to represent the line by a distributed *RLC* model whose parameters are obtained from T line equations or field simulators (Fig. 7). The principal difficulty in such a transformation relates to the modeling of

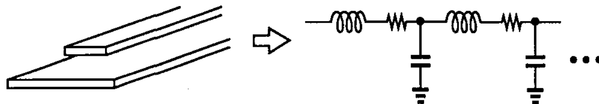

Fig. 7. Distributed circuit representation of a T line.

the skin-effect loss in broadband circuits. With signal bands spanning many frequency decades, it becomes necessary to include different resistances in the model that manifest themselves at different frequencies. As a simple example, consider including both the dc resistance and the 40-GHz skin-effect resistance of the geometry shown in Fig. 3. If both resistances are merged into a series component in the distributed model (as in Fig. 7), then the circuit displays an unrealistic behavior in some cases. In particular, if the T line serves as a load inductor in an oscillator (Fig. 8), the series representation predicts that the Q of the line increases *linearly* with frequency. For example, with an oscillation frequency of 40 GHz, the artificial rise in the Q at the odd harmonics (120 GHz, 200 GHz, etc.) leads

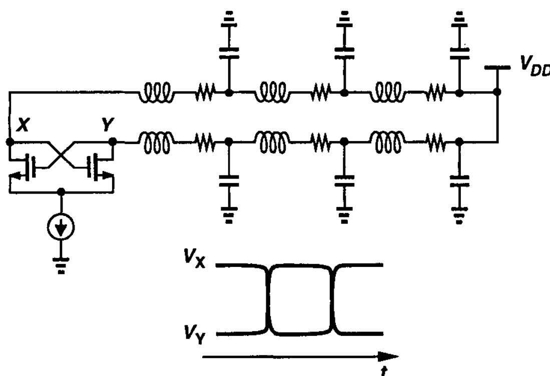

Fig. 8. Oscillator using T lines as inductors.

to sharp edges in the simulated output waveforms and hence unrealistically short rise and fall times.

The above artifact necessitates modeling the loss as a parallel resistor but such a representation fails to account for the low-frequency resistance of the wire (Fig. 9), a critical issue if the line is loaded by a termination resistor, thereby suffering from

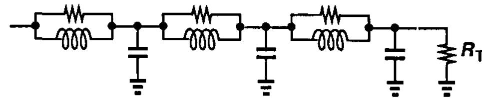

Fig. 9. Distributed T line model with termination resistance.

dc voltage attenuation. Thus, both series and parallel resistors are necessary.

General modeling of the skin effect extends the above ideas to more parallel branches [4]. Depicted in Fig. 10(a) for a coaxial cable, this approach views the signal line as a set of

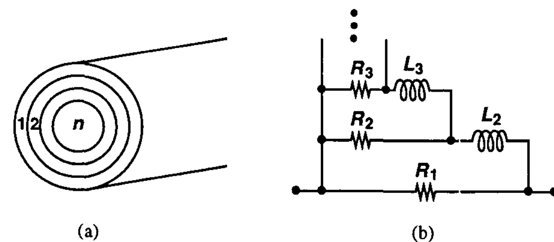

Fig. 10. (a) View of a conductor at high frequencies, (b) resulting model.

concentric cylinders, each having some (low-frequency) resistance and inductance, arriving at the circuit in Fig. 10(b) for one section of the distributed model. Here, the branch consisting of R_j and L_j represents the impedance of cylinder number j. At low frequencies, the current is uniformly distributed through the conductor and the model is reduced to $R_1||R_2||\cdots||R_n$ [4]. As the frequency increases, the current moves away from the inner cylinders, an effect modeled by the rising impedance of the the inductors in each branch. In [4], a constant ratio R_j/R_{j+1} is maintained to simplify the model while achieving a reasonable agreement between the simulated and measured transient behavior of T lines.

The key feature of the above method is that it reduces the problem of skin effect to the calculation of low-frequency resistances and inductances. However, the approach is more difficult to apply to microstrips as it requires computing the inductance of a rectangular pipe lying on top of a ground plane (Fig. 11). Field simulators therefore prove essential here.

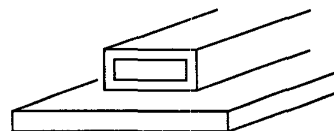

Fig. 11. Part of a microstrip for skin effect calculations.

IV. T Lines as Circuit Elements

A. Small Inductors

A T line shorted at the far end exhibits an inductive input impedance if its length, l, is less than a quarter of the wavelength, λ. The input impedance is then given by

$$Z_{in} = j \tan \frac{2\pi}{\lambda} l, \qquad (16)$$

which, for $2\pi l/\lambda \ll 1$ rad, yields:

$$L_{eq} \approx \frac{Z_0 l}{v}. \qquad (17)$$

This result is of course to be expected because, with $Z_0 = \sqrt{L_u/C_u}$ and $v = 1/\sqrt{L_u C_u}$, it predicts $L_{eq} = L_u \cdot l$. In the example of Fig. 3, a microstrip 1 mm long provides an inductance of 523 pH with a skin resistance of 9.35 Ω at 40 GHz, i.e., a Q of 14.

An important advantage of inductive T lines over spiral inductors stems from the accuracy with which the former's parameters can be calculated. Unlike spiral geometries, microstrips exhibit confined fields, thereby producing negligible eddy currents in the substrate and allowing precise calculation of inductance and loss.

B. Controlled-Impedance Interconnects

In some cases, it is possible to configure a long interconnect as a T line having a desirable characteristic impedance, thereby obviating the need to deal with the wire as a large parasitic capacitance or inductance. In particular, input and output stages that interface a circuit with the off-chip environment can benefit from T-line interconnects.

Consider a broadband input differential pair incorporating inductive peaking. As illustrated in Fig. 12, the large dimensions of spiral inductors inevitably lead to long interconnects at the input or output of the stage. We note that in Fig. 12(a), the input lines can be designed as shown in Fig. 5 to match the termination resistance R_T, thereby minimizing reflections at the input. In Fig. 12(b), on the other hand, it is difficult to match the long wires to the termination impedance consisting of R_P, L_P, and C_L. As a result, the interconnects degrade the circuit's broadband response considerably. Thus, the configuration in Fig. 12(a) is preferable.

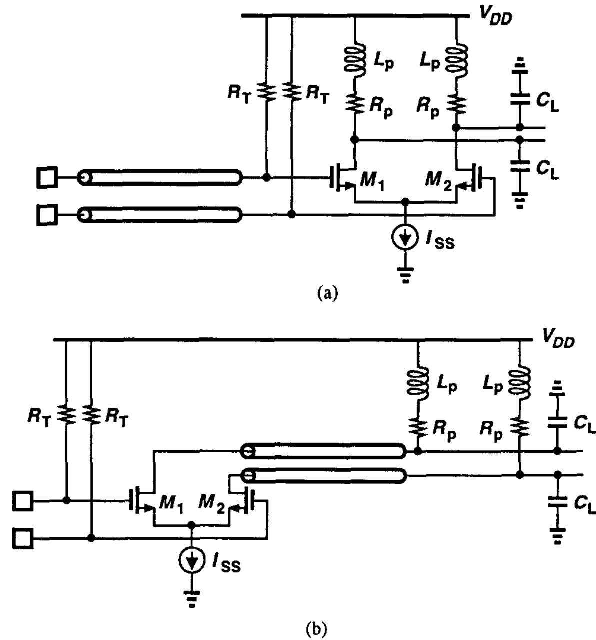

Fig. 12. Possible configurations for routing input lines to a differential pair using inductive peaking.

A similar situation arises in output stages. Figure 13 depicts two possible configurations for placing a doubly-terminated output stage between a predriver and output pads. In Fig. 13(a), the output stage lies near the pads, loading the predriver with long interconnects and degrading the speed. In Fig. 13(b), the output differential pair is close to the predriver and the output interconnects are designed for a characteristic impedance equal to R_T. The latter is preferable because it ensures reasonable impedance matching seen in both forward and reverse directions.

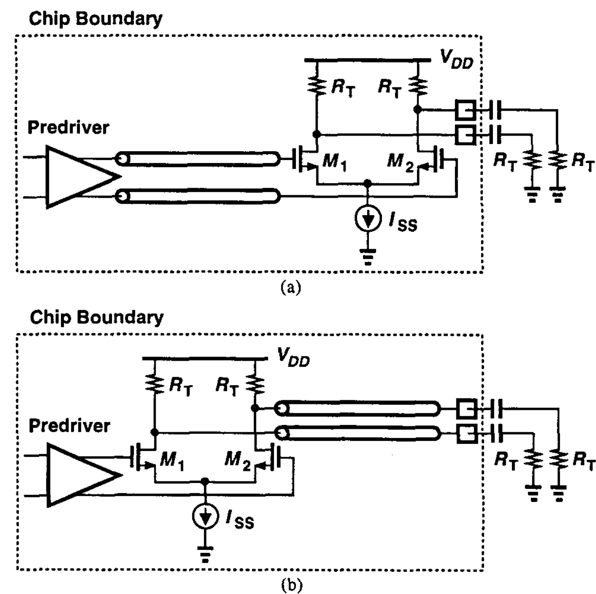

Fig. 13. Possible configurations for routing the output lines to pads.

C. Electrostatic Discharge Protection

Circuits operating at gigahertz speeds require electrostatic discharge (ESD) protection devices that exhibit a small capacitance. However, the trade-off between the capacitance and the maximum tolerable voltage of typical ESD structures compromises the packaging and handling yield.

It is possible to embed ESD devices in a transmission line so as to achieve both impedance matching and a high voltage tolerance [5]. Illustrated in Fig. 14, the idea is to distribute the ESD structure consisting of the NMOS and PMOS devices over a T line so that only the characteristic impedance decreases but other properties remain intact. For example, to

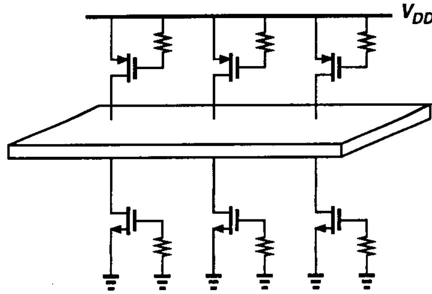

Fig. 14. Distributed ESD structure.

lower the value of Z_0 for the microstrip in Fig. 3 from 94.3 Ω to 50 Ω, the capacitance per unit length can increase from 58.8 fF/mm to 307 fF/mm. Thus, an ESD capacitance of 248 fF can be added to every millimeter of the line.

The technique of Fig. 14 entails several issues. First, to accommodate sufficient ESD capacitance (e.g., 1 pF), the microstrip line must be quite long, occupying a large area and, more importantly, introducing substantial loss. Second, the junction diodes of the ESD MOSFETs typically suffer from a large series resistance, further increasing the loss of the T line.

V. CIRCUIT APPLICATIONS

A. Distributed Amplifiers

Distributed amplification in principle overcomes the trade-off between gain and bandwidth [6]. Illustrated in Fig. 15, a simple distributed amplifier (DA) incorporates two T lines,

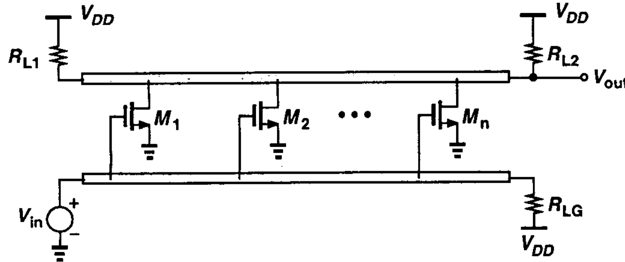

Fig. 15. Simple distributed amplifier.

one for the input and another for the output. The capacitances contributed by each transistor decrease both the characteristic impedance and the wave velocity. We denote the loaded values by Z_{0L} and v_{0L}, respectively, assuming that the loaded input and output lines exhibit equal parameters. Note that if V_{in} steps up by ΔV, then each transistor draws a current equal to $g_m \Delta V$, generating a drain voltage step of $g_m \Delta V Z_{0L}/2$ that travels toward R_{L2}. If the wave velocities of the input and output lines are equal, then each transistor senses the input step at exactly the same time as the output step produced by the preceding transistor(s) arrives at its drain. Since the waves reaching the ends of both lines are absorbed by R_{L1}, R_{L2}, and R_{LG}, no reflections corrupt the signal.

With lossless T lines, the DA of Fig. 15 provides infinite gain with infinite bandwidth: each common-source (CS) stage along with an additional length of T line increases the gain by $g_m Z_{0L}/2$. To quantify this ideal behavior, suppose a DA employs n CS stages distributed over a line of length l. Neglecting Miller effect and line loss and assuming that the output line is loaded such that it exhibits the same characteristics as the input line, we express the capacitance per unit length as $C_{uL} = C_u + nC_{GS}/l$. Thus,

$$Z_{0L} = \sqrt{\frac{L_u}{C_u + \frac{nC_{GS}}{l}}}, \tag{18}$$

yielding a total voltage gain of

$$A_v = \frac{ng_m}{2}\sqrt{\frac{L_0}{C_0 + \frac{nC_{GS}}{l}}}. \tag{19}$$

In the ideal case, the capacitance of the line itself is much less than nC_{GS}/l. Also, it is common to write for a MOSFET $\omega_T \approx g_m/C_{GS} \approx g_m/(WLC_{ox})$. Therefore, A_v is simplified to

$$A_v \approx \pi f_T \frac{l}{v}, \tag{20}$$

where l/v signifies the end-to-end delay of the line.

The performance of distributed amplifiers is constrained by five effects. First, the limited supply voltage places an upper bound on the number of the CS stages and hence the achievable voltage gain. Second, resistive losses in the input T lines gradually attenuate the signal applied to the gates of the transistors, leaving little amplitude for the stages near the far end. Third, as in passive T lines, resistive losses limit the bandwidth in both the input and the output networks. Fourth, the output resistance of the transistors raises the loss in the output T line. Fifth, the Miller multiplication of each transistor's gate-drain overlap capacitance becomes more significant as the wave travels toward the far end. This is because, in Fig. 15, the apparent voltage gain from the gate to the drain of M_n is n times that seen by M_1.

Let us now determine how the number of sections must be chosen in the presence of loss in the input T line. Suppose each section incorporates a transistor with transconductance g_m and a line of length l_u. Since the input signal amplitude drops by a factor of $\exp(-\alpha k l_u)$ after k sections, where α denotes the loss, we express the total gain resulting from n sections as

$$A_v = \sum_{k=0}^{n-1} e^{-\alpha k l_u} \frac{g_m Z_{0L}}{2} \tag{21}$$

$$= \frac{1 - e^{-\alpha n l_u}}{1 - e^{-\alpha l_u}} \frac{g_m Z_{0L}}{2}. \tag{22}$$

In a well-designed DA, it is reasonable to assume $\alpha n l_u < 0.5$, allowing the approximation $\exp \epsilon \approx 1 + \epsilon + \epsilon^2/2$ for both the numerator and the denominator of the first fraction in (22):

$$A_v \approx n \frac{1 - \frac{\alpha n l_u}{2}}{1 - \frac{\alpha l_u}{2}} \frac{g_m Z_{0L}}{2}. \tag{23}$$

As expected, if $\alpha \to 0$, then A_v approaches $ng_m Z_{0L}/2$. Since $\alpha l_u \ll 1$, we assume $1/(1-\epsilon) \approx 1+\epsilon$ and rewrite (23) as

$$A_v \approx n(1-\alpha l_u \frac{n-1}{2})\frac{g_m Z_{0L}}{2}, \quad (24)$$

where the second-order term is neglected.

Equation (24) reveals that as n increases, the term in the parentheses slows down the growth of the gain. Of course, with the assumption $\alpha n l_u < 0.5$ made earlier, the factor $1 - \alpha l_u(n-1)/2$ at most falls to 0.75. Now suppose we choose n such that this term is equal to 0.8:

$$1 - \alpha l_u \frac{n-1}{2} = 0.8, \quad (25)$$

obtaining the number of sections as:

$$n = \frac{0.4}{\alpha l_u} + 1. \quad (26)$$

For example, if $\alpha l_u = 0.1$, then $n = 5$ and $n[1-\alpha l_u(n-1)/2] = 4$. With this value of αl_u, if n is raised to 6, then $n[1-\alpha l_u(n-1)/2] = 4.5$, a relatively small increase.

The output resistance of short-channel MOSFETs biased at high currents can increase the loss of the *output* T line in a distributed amplifier. Appearing from each drain node to ground, such resistance leads to the following loss expression:

$$\alpha = \frac{R_{skin}}{2Z_0} + \frac{mZ_0}{2r_O}, \quad (27)$$

where it is assumed m transistors, each having an output resistance of r_O, are used per unit length of the T line. If in the above example, five transistors are used per millimeter, then r_O must exceed 47.5 kΩ if it must not increase α by more than 10%. In reality, r_O falls in the range of 5 to 10 kΩ, raising the loss substantially.

If a distributed amplifier is driven by an on-chip circuit, then its input impedance loads the preceding stage, possibly degrading the overall gain of the cascade. Modeling the cascade as shown in Fig. 16, we note that the output voltage of the DA is equal to $I_1 Z_{0L} A_v$, concluding that it is the *product* of

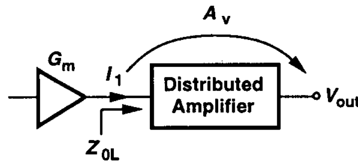

Fig. 16. Cascade of a predriver and a distributed amplifier.

Z_{0L} and A_v that ultimately determines the gain of the overall circuit. From this perspective,

$$A_v Z_{0L} \approx \pi f_T \frac{l}{v} Z_{0L} \quad (28)$$

$$= \pi f_T l L_u. \quad (29)$$

Interestingly, for a given f_T, the product is independent of the transistor gate-source capacitance, suggesting that L_u must be maximized.

The problem of Miller multiplication, voltage headroom, and T line loss can be alleviated by cascading two or more distributed amplifiers. Illustrated in Fig. 17, such a cascade allows the output current of the first DA to flow through the

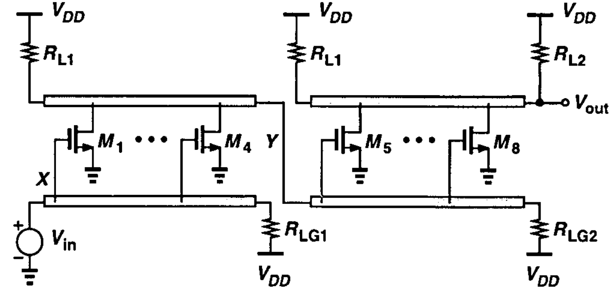

Fig. 17. Cascaded distributed amplifiers.

input T line of the next. Since each DA incorporates only a few sections, the above effects do not accumulate through the chain. Unfortunately, the drain bias voltage of M_1-M_4 must be high enough to provide the gate-source voltage required for M_5-M_8, further limiting the voltage drop across $R_{L1}||R_{LG12}$ and hence the gain. Without M_5-M_8, the first DA could allow V_Y to be lower than V_X by one MOS threshold voltage, a substantial difference in voltage headroom.

Unlike conventional microwave and millimeter-wave circuits, modern high-speed systems require differential implementations of distributed amplifiers (Fig. 18). The large

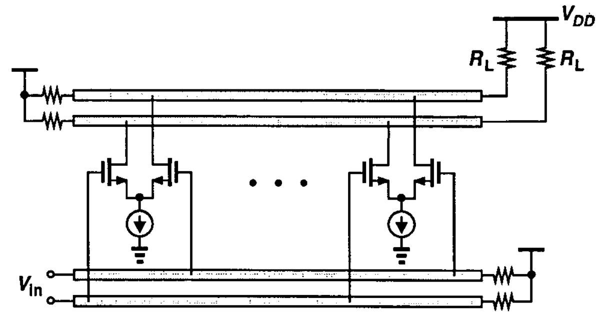

Fig. 18. Differential distributed amplifier.

spacing required between the input and output lines to ensure minimal coupling leads to a large and complex layout.

B. Distributed Oscillators

A distributed amplifier can be placed in a feedback loop to form an oscillator (Fig. 19) [7, 8]. To this end, the total delay of the inverting amplifier must translate to a phase shift of 180° at the frequency of interest, f_{osc}. This is guaranteed if $l/v = 1/(2f_{osc})$, which, for the idealized scenario described in the previous section, yields

$$A_v = \frac{\pi f_T}{2f_{osc}}. \quad (30)$$

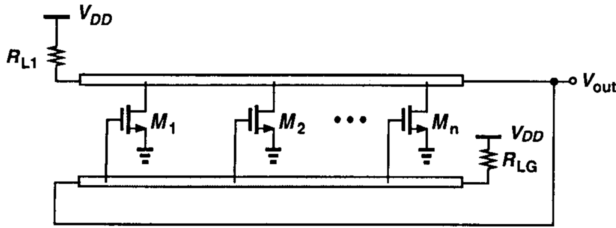

Fig. 19. Distributed oscillator.

For a minimum loop gain of unity, (30) gives

$$f_{osc} = \frac{\pi}{2} f_T, \qquad (31)$$

indicating potential for very high oscillation frequencies. For example, a 0.13-μm NMOS device with reasonable overdrive voltage exhibits an f_T of roughly 70 GHz, enabling distributed oscillators to run at speeds greater than 100 GHz.

The five limiting factors outlined in the previous section for DAs also impact the performance of distributed oscillators. With typical T lines available in CMOS technology, oscillation frequencies on the order of half of that predicted by (31) can be achieved.

C. Rotary Traveling-Wave Oscillator

An interesting application of T lines to clock distribution in large digital systems is based on the "rotary traveling-wave oscillator" (RTWO) concept [9]. Illustrated in Fig. 20, an RTWO incorporates a T line that is wrapped around, with its

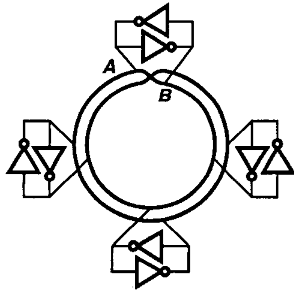

Fig. 20. Rotary oscillator [9].

input and output shorted together. The line is stimulated into oscillation by cross-coupled inverters distributed around the ring. The oscillation frequency is given by the wave velocity of the loaded line and the total length from A to B in the direction of wave travel.

An array of rotary oscillators can form a clock distribution network that provides identical phases across a large chip. As depicted in Fig. 21, 25 interconnected RTWOs yield 25 locations across the chip carrying in-phase clock signals.[2]

For phase-locking purposes, the rotary oscillator must employ means of tuning the frequency. MOS varactors can be placed next to each cross-coupled pair so as to load the T lines uniformly, but routing the control line to all such locations

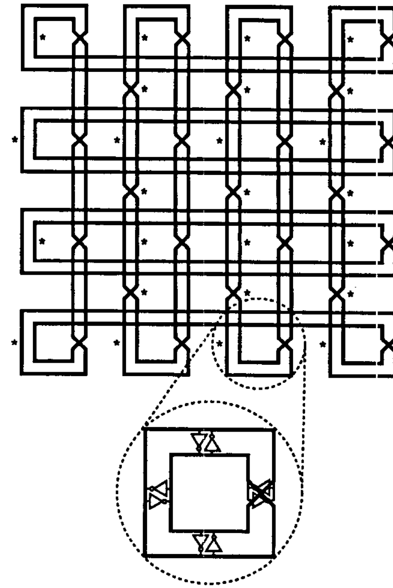

Fig. 21. Array of rotary oscillators [9].

across the chip potentially leads to substantial noise coupling from the environment and hence a large jitter.

[2]The actual design employs more cross-coupled pairs per ring than shown in Fig. 21.

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