Architectures and Circuits for RF CMOS Receivers

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Abstract

This paper presents recent work in receiver architectures and circuits for RF CMOS applications. First, receiver topologies such as heterodyne, direct-conversion, and image-reject configurations together with their trade-offs are described. Next, the design of building blocks, e.g., low-noise amplifiers and mixers, baseband interfaces, and oscillators is studied. Three design examples for ISM, DECT, and cellular applications are then reviewed and unresolved issues in RF CMOS design are summarized.

I. INTRODUCTION

The RF CMOS fever continues to spread. While MOSFETs were considered noisy, slow devices up to about a decade ago, scaling has dramatically improved their performance, achieving transit frequencies of tens of gigahertz in the 0.35-μm generation and suggesting the feasibility of RF CMOS circuits in the range of a few gigahertz. The lower cost and faster advance of CMOS processes with respect to silicon and III-V technologies has motivated extensive efforts in designing RF CMOS circuits.

CMOS technologies exhibit properties and limitations that directly impact the design of a receiver from the architecture level to the device level and from the antenna to the baseband processor. Thus, "concurrent engineering" plays an important role in the overall performance and the time to market of such products.

This paper describes the design of RF receivers at architecture and circuit levels in CMOS technology. Section II reviews receiver architectures, including heterodyne, direct-conversion, and image-reject techniques. Section III deals with the design of building blocks such as low-noise amplifiers (LNAs), mixers, baseband interfaces, oscillators, and quadrature generators. Section IV reviews three design examples for ISM, DECT, and cellular systems and Section V summarizes present difficulties in RF CMOS design.

II. RECEIVER ARCHITECTURES

Complexity, cost, power dissipation, and the number of external components have been the primary criteria in selecting receiver architectures. As IC technologies evolve, however, the relative importance of each of these criteria changes, allowing approaches that once seemed impractical to return as plausible solutions. Since filter requirements prohibit channel selection at RF, receivers first translate the input spectrum to a much lower frequency.

A. Heterodyne Receivers

Heterodyne receivers downconvert the input to an "intermediate frequency" (IF), perform band-pass filtering and amplification, and translate the spectrum to a lower frequency again (Fig.1). In the case of phase or frequency modulation,
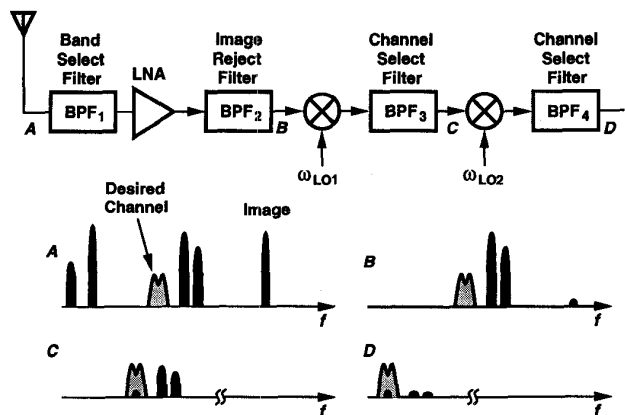

Fig. 1. Dual-conversion heterodyne receiver.

downconversion to the baseband requires both in-phase (I) and quadrature (Q) components of the signal. This is because the two sidebands of such signals carry different information and must be separated into quadrature phases in translation to zero frequency.

Perhaps the most important feature of the heterodyne receiver is its selectivity, i.e., the capability to process and select small signals in the presence of strong interferers. While selecting a 30-kHz channel at a center frequency of 900 MHz requires prohibitively large Q's, in Fig. 1 band-pass filtering is performed at progressively lower center frequencies.

Heterodyning nonetheless entails a number of drawbacks. The trade-off between image rejection and channel selection typically requires a relatively high IF, making it difficult to integrate the IF filter monolithically. Furthermore, the image-reject filter is a passive, bulky device that must be placed off-chip and driven as a 50-Ω load. This intensifies the trade-offs in the design of the low-noise amplifier.

In heterodyne architectures, the choice of the noise figure (NF), the third intercept point (IP_3), and the gain of each stage in the chain depends on those of the preceding and fol-

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lowing stages, thereby demanding considerable iteration at the architecture and circuit levels to arrive at an acceptable distribution of gain in the receiver building blocks. Moreover, each mixer generates many spurious components whose frequencies are related to those of the RF and IF signals and the oscillators. Some of these components may fall in the desired channel, degrading the signal quality. Thus, the "frequency planning" of the receiver directly impacts the performance of the receiver in the presence of interferers.

B. Direct-Conversion Receivers

Direct-conversion receivers translate the channel of interest directly to zero frequency (Fig. 2). For frequency- and phase-modulated signals, the downconversion must provide quadrature outputs so as to avoid loss of information.
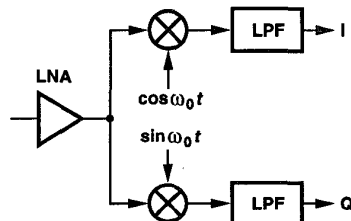
Fig. 2. Direct-conversion receiver.

Direct conversion offers two important advantages over a heterodyne counterpart. First, the problem of image is circumvented because $\omega_{IF} = 0$. As a result, no image filter is required and the LNA need not drive a 50-Ω load. Second, the IF filter and subsequent downconversion stages are replaced with low-pass filters and baseband amplifiers that are amenable to monolithic integration.

The simplicity of direct conversion nevertheless comes with a number of design issues. First, as shown in Fig. 3, dc offsets due to mixing of the local oscillator (LO) leakage with itself
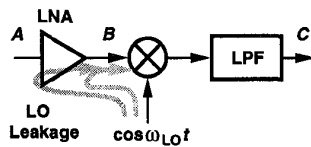
Fig. 3. DC offset due to self-mixing of LO.

corrupt the baseband signal and, more importantly, saturate the following gain stages [1, 2]. At the output of the mixer, such offsets can be as high as 10 mV whereas the signal may be as low as a few tens of microvolts. If the modulation scheme contains significant energy near dc, as is the case in most cellular and cordless phone standards, then ac coupling with practical values of capacitors and time constants severely degrades the signal. To remove dc offsets, periodic offset cancellation can be performed during idle times, but at the cost of kT/C noise [1].

Second, as depicted in Fig. 4, even-order distortion in the RF signal path generates low-frequency beats from large interferers. In the presence of mismatches and hence asymmetry in the mixer, such components appear at the output, thus degrading the signal-to-noise ratio (SNR). This effect can be reduced
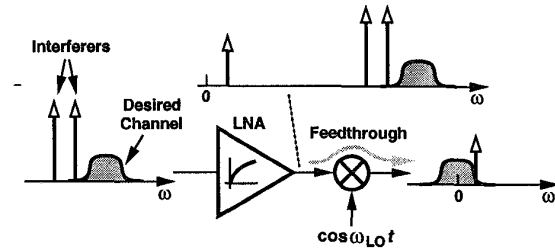
Fig. 4. Effect of second-order distortion in direct-conversion receivers.

by differential circuits or high-pass filtering the beats.

Owing to the limited gain provided by the LNA and the mixer, the downconverted signal is quite sensitive to noise. Especially problematic here is the flicker noise of baseband amplifiers and filters in CMOS technology, making it desirable to realize a *high* gain in the RF and IF sections.

Another issue in direct-conversion receivers is the phase and gain mismatch introduced by the mixers. As shown in Fig. 5, phase mismatch gives rise to *cross-talk* between demodulated
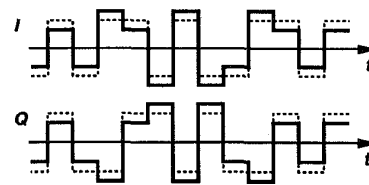
Fig. 5. Effect of I/Q phase imbalance on demodulated QPSK data.

quadrature waveforms, lowering the SNR because the I and Q data streams are usually uncorrelated.

In addition to the above issues, the leakage of the LO signal to the antenna creates interference in the band of other users and must therefore be sufficiently small (typically between −60 and −80 dBm).

While most of these difficulties can be resolved by means of circuits techniques, the dc offset and flicker noise problems continue to challenge designers.

C. Image-Reject Architectures

The issues related to the image-reject filter have motivated RF designers to seek other techniques of rejecting the image in a heterodyne receiver. One such technique originates from a single-sideband modulator introduced by Hartley [3]. Illustrated in Fig. 6, Hartley's circuit mixes the RF input with the
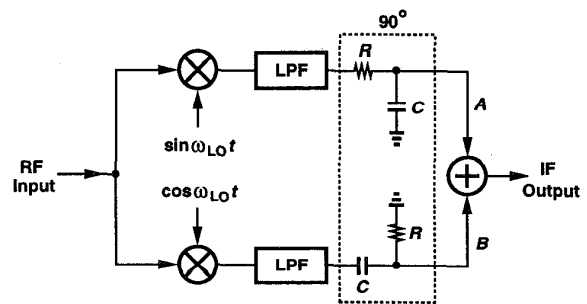
Fig. 6. Hartley image-reject receiver.

quadrature outputs of the local oscillator, low-pass filters and

shifts the results by 90° before adding them together. It can be shown that the spectra at points A and B contain the desired band with the same polarity and the image with opposite polarity. The summed output is therefore free from the image.

The principal drawback of the Hartley architecture is its sensitivity to mismatches: with phase and gain imbalance, the image is only partially cancelled. Note that the effect of I/Q mismatch is much more severe here than in direct-conversion topologies. Also, the loss and noise of the shift-by-90° stage and the linearity of the adder are critical parameters. Furthermore, the variation of R and C introduces gain mismatch, limiting the image rejection ratio severely.

Shown in Fig. 7 is another image-reject architecture introduced by Weaver [4]. Replacing the 90° shift of Hartley's cir-
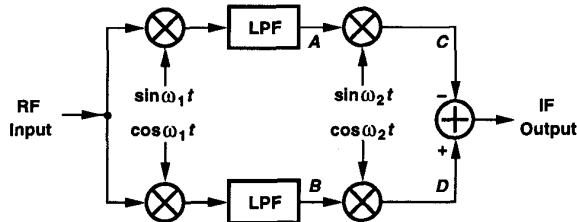

Fig. 7. Weaver image-reject receiver.

cuit with a second quadrature mixing operation, this technique provides an arbitrary translation of the signal band without image interference. It can be shown that the subtraction of the spectrum at point C from that at point D produces the signal while suppressing the image.

The Weaver architecture is also sensitive to mismatches, but it avoids the use of an RC-CR network, thereby achieving greater image rejection despite process and temperature variations.

D. Digital-IF Receivers

In the dual-conversion heterodyne architecture of Fig. 1, low-frequency operations such as the second set of mixing and filtering can be performed more efficiently in the digital domain. Shown in Fig. 8 is an example where the first IF signal
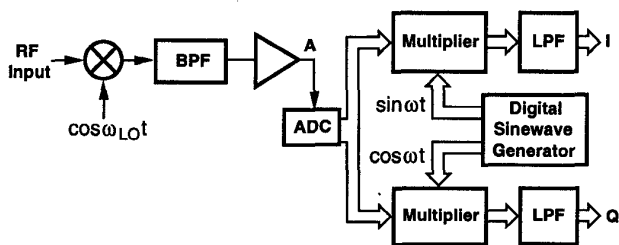

Fig. 8. Digital-IF receiver.

is digitized, "mixed" with the quadrature phases of a digital sinusoid, and low-pass filtered to yield the quadrature baseband signals. This approach is sometimes called a "digital-IF architecture." Note that digital processing avoids the problem of I and Q mismatch.

The principal issue in this approach is the performance required of the A/D converter. Since the signal level at point A

in Fig. 8 is typically no higher than a few hundred microvolts, the quantization and thermal noise of the ADC must not exceed a few tens of microvolts. Furthermore, if the first IF bandpass filter cannot adequately suppress adjacent interferers, the nonlinearity of the ADC must be sufficiently small to minimize corruption of the signal by intermodulation. Additionally, the ADC must achieve an input bandwidth commensurate with the value of IF while consuming a reasonable amount of power.

The above requirements make it difficult to employ a Nyquist-rate ADC in the digital-IF architecture. Typical IF values of 50 to 200 MHz mandate sampling rates in the range of 100 to 400 MHz, and linearity, noise floor, and dynamic range requirements may necessitate resolutions greater than 14 bits. Such performance cannot be obtained in today's A/D converters even if cost and power dissipation are not critical. The idea is nonetheless the subject of active research [5, 6].

III. BUILDING BLOCKS

RF architectures impose severe requirements upon the performance of their constituent circuits. The very small signal amplitude received by the antenna in the presence of large interferers mandates both careful allocation of noise and linearity to various stages and sufficient suppression of spurious components generated in the frequency synthesizers and the power amplifier.

As with most analog systems, RF circuits suffer from trade-offs among various parameters. We illustrate such trade-offs in an "RF design hexagon" (Fig. 9), where almost every two parameters trade each other. The hexagon also indicates that
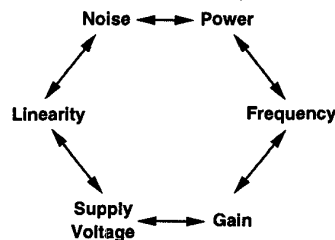

Fig. 9. RF design hexagon.

simple figures of merit such as f_T, f_{max}, and gate delay cannot be easily used to predict RF performance because they do not reflect many of the trade-offs.

A. LNAs and Downconversion Mixers

As the first stages to handle the received band, LNAs and downconversion mixers carry the heaviest burden in terms of noise and linearity. In a typical heterodyne front end (Fig. 1), the band-select filter introduces a loss of 2 to 3 dB, in effect "magnifying" the noise of the LNA by the same amount when it is referred to the antenna port. Furthermore, the LNA must drive the 50-Ω input impedance of the image reject filter while providing a reasonable gain. It is important to note that the LNA gain must be chosen according to the noise and linearity of the mixer. If this gain is too low, the mixer noise dominates the overall noise figure, and if it is too high, the input signal to the mixer creates large intermodulation products.

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The very low noise required of the LNA usually mandates the use of only one active device at the input without any (high-frequency) resistive feedback. In addition to the RF design hexagon, a number of other considerations govern the design of low-noise amplifiers. For example, input matching to 50 Ω is necessary because the band-pass filter following the antenna is designed to be used in various receiver systems and must therefore operate with a standard termination impedance. If the source and load impedances seen by the filter deviate from 50 Ω significantly, then the pass-band and stop-band characteristics of the filter may exhibit considerable loss and ripples.

Noise, input matching, and stability requirements limit acceptable LNA topologies to only a few. Widely used are common-gate and inductively-degenerated cascode topologies (Fig. 10) as they provide both a high reverse isolation (thus en-
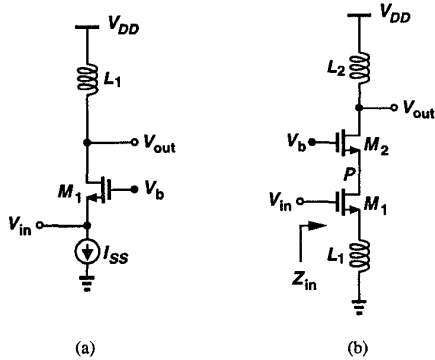

Fig. 10. (a) Common-gate and (b) cascode LNAs.

suring stability) and an input resistance that can be set to 50 Ω by design. If the drain noise current of M_1 in Fig. 10(a) is expressed as $I_n^2 = 4kT\gamma g_m$ (where $\gamma = 2/3$ for long-channel devices), the noise figure is given by $NF = 1 + \gamma$ [7]. For $\gamma = 2/3$, $NF = 5/3 = 2.2$ dB. While this suggests a reasonable noise figure for matched-input common-gate topologies, in reality other sources of noise degrade the performance substantially. In short-channel MOSFETs, the factor γ may be quite higher than 2/3 [8]. Furthermore, the bias current source and possibly the load generate additional noise.

The cascode circuit of Fig. 10(b) incorporates inductive degeneration to create a real part in the input impedance. Neglecting the gate-drain and source-bulk capacitance, we can write:

$$Z_{in} \approx \frac{g_{m1}L_1}{C_{GS1}} + L_1s + \frac{1}{C_{GS1}s}. \quad (1)$$

Thus, proper choice of g_{m1}, L_1, and C_{GS1} yields a 50-Ω real part. In practice, the last two terms may not resonate at the frequency of interest, necessitating the use of off-chip components at the input. At high frequencies, the required value of L_1 becomes comparable with the inductance of the ground bond wire, requiring multiple bonds or accurate modeling of the wire inductance. Also, the reduction of the equivalent transconductance as a result of degeneration may magnify the noise contributed by M_2. This is because the parasitic capacitance at node P provides some gain from the gate of M_2 to

the output.

Common-gate and cascode topologies have also been utilized in differential form [9, 10, 11]. While differential operation lowers the sensitivity to common-mode disturbance, it requires higher power dissipation to achieve the same noise figure as a single-ended counterpart. More importantly, if the signal generated by the antenna is single-ended, a means of conversion to differential form, e.g., a transformer, is necessary. However, on-chip transformers exhibit a prohibitively high loss and off-chip devices are bulky and/or expensive.

The IP_3 of CMOS common-gate and cascode LNAs is quite high, typically greater than -5 dBm if noise and matching requirements are met. Thus, the linearity of the subsequent stages tends to be the limiting factor. In particular, the down-conversion mixer(s) must achieve high linearity and a reasonable noise figure. Fig. 11 shows single-balanced and double-balanced mixer topologies. For a given supply current, the circuit of Fig. 11(a) exhibits less input noise than that in Fig.
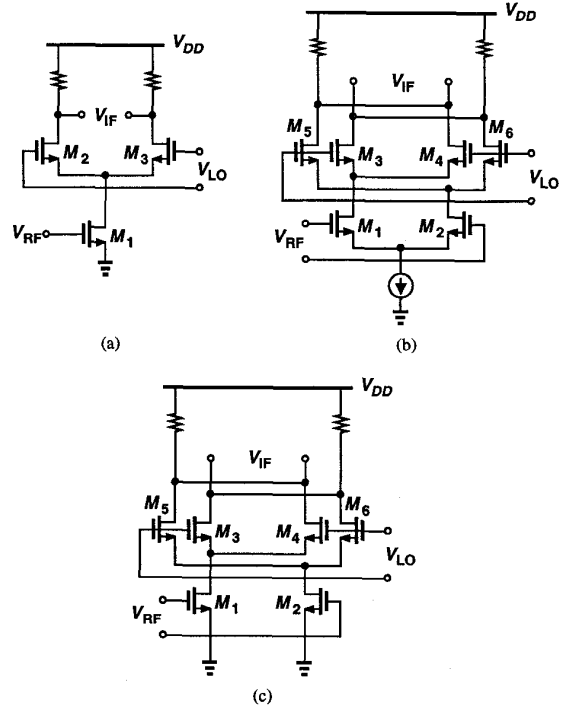

Fig. 11. (a) Single-balanced mixer, (b) double-balanced mixer, (c) mixer of (b) with grounded-source input stage.

11(b). However, the double-balanced topology entails much less LO-IF feedthrough and suppresses the effect of additive noise in the LO input.

Two properties of active CMOS mixers distinguish their design from their bipolar counterparts: the linearization procedure and the required LO drive. In Fig. 11(a), M_1 can be linearized by simply increasing the gate-source overdrive voltage, $V_{GS} - V_{TH}$, with no need for explicit degeneration. This of course trades with the bias current or the transistor aspect ratio, raising the power consumption or lowering the device transconductance. In Fig. 11(b), on the other hand, the inter-

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action between M_1 and M_2 through their common source node gives rise to substantial third-order nonlinearity. By contrast, if the sources of M_1 and M_2 are grounded [Fig. 11(c)], a much higher IP_3 is obtained.

CMOS mixers typically demand large LO swings so that the switching pairs [e.g., M_2 and M_3 in Fig. 11(a)] do not remain on simultaneously for a considerable period of time. Increasing the width of the switching devices can lower the required swing, but at the cost of increasing their noise contribution and higher capacitance in the RF signal path. Thus, the choice of device dimensions and bias currents plays a critical role in the performance.

Passive CMOS mixers have also been used [10] (Fig. 12). Since the circuit exhibits a loss of several decibels, a low-
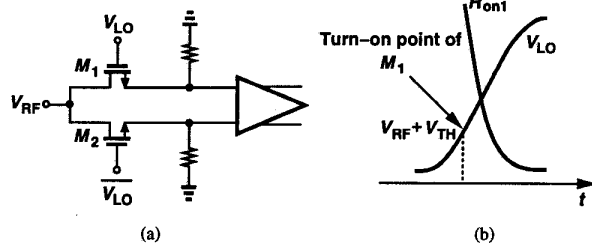

Fig. 12. (a) Passive mixer with low-noise stage, (b) generation of nonlinearity as one device turns off.

noise stage must follow the mixer. This is also necessary if the outputs of two mixers are to be added (e.g., Fig. 7). While passive mixers are considered more linear than active implementations, it is unclear whether the combination of the mixer core and the subsequent amplifier offers a more relaxed noise-linearity-power trade-off than the active circuits of Fig. 11. As shown in Fig. 12(b), with sinusoidal LO signals, the switches have a relatively small gate-source overdrive voltage for a significant part of the period. Thus, the RF input greatly varies the switch on-resistance during this time, introducing distortion.

The interface between the LNA and the mixer merits particular attention. While in heterodyne receivers employing external image-reject filters, a 50-Ω, ac-coupled interface connects the LNA to the filter and subsequently to the mixer, in other architectures the impedance level and the type of coupling are flexible. Fig. 13 illustrates three implementations of the interface. In Fig. 13(a), the two stages are capacitively coupled and the mixer input stage is biased by means of M_0 and I_{REF}. Resistor R_b is much greater than the output impedance of the LNA. This approach suffers from signal loss due to the bottom-plate parasitic of C_1.

In Fig. 13(b), the interface consists of a common-source stage, M_1, with the bias current defined by I_b and an ac short provided by C_1 [12]. The small-signal drain current of M_1 is drawn from the switching pair through C_2, whose parasitic capacitance resonates with L_2. The signal loss due to the parasitic of C_2 in this case occurs after substantial amplification, thereby influencing the overall noise figure to a lesser extent. Note that the drain noise current of M_2 is reduced by inductive degeneration.
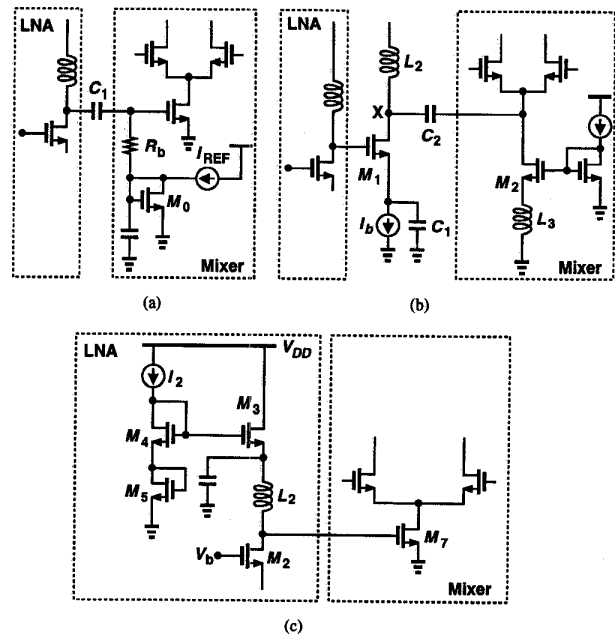

Fig. 13. Interfaces between LNA and mixer.

In Fig. 13(c), the LNA incorporates the dc load M_3 with current mirrors M_4 and M_5 [13]. Neglecting the dc drop across L_2, we note that $V_{GS5} + V_{GS4} = V_{GS3} + V_{GS7}$. Thus, proper ratioing of M_3 and M_7 with respect to M_4 and M_5 defines I_{D7} as a multiple of I_2. This approach incurs no signal loss but consumes voltage headroom.

B. Baseband Interface

The design of receiver baseband circuits becomes progressively more difficult as the RF and IF sections of receivers incorporate fewer external components and hence perform a lesser portion of the signal processing task. More specifically, in order to allow simpler image rejection, the first IF has in recent years increased from a relatively common value of 10.7 MHz to much higher values [14, 15], thereby mandating that channel-selection filtering be moved from the first IF to the baseband. Fig. 14 depicts an example [14]. Furthermore,
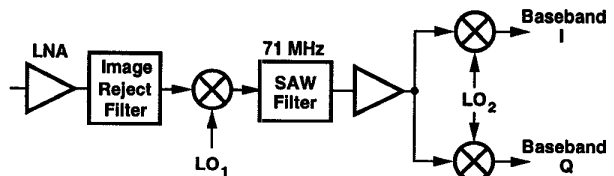

Fig. 14. Typical heterodyne receiver chain [14].

noise-linearity-power trade-offs limit the amount of gain provided by the RF and IF circuits. As a result, the baseband section must process small signals in the presence of large interferers. It is interesting to note that this trend creates most of the direct-conversion drawbacks in heterodyne topologies as well. In particular, the processing following the first IF in Fig. 14 entails dc offsets due to self-mixing of the second LO,

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flicker noise, I/Q mismatch, and second-order distortion.

After the signal is downconverted to the baseband, it must be filtered, amplified, and digitized, but not necessarily in that order. Consider the interface between the mixer and the first baseband stage (Figure 15). We make two observations. First,
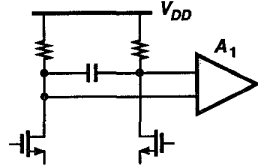

Fig. 15. Interface between mixer and following stage.

at this point the signals are still quite small (in the range of tens of microvolts) and the interferers quite large (e.g., 60 dB above the signal level). Thus, both the noise and the nonlinearity of A_1 are critical. Second, to avoid lowering the voltage gain of the mixer, A_1 must exhibit a relatively high input impedance.

With the above in mind, let us study the three permutations depicted in Figure 16. In Figure 16(a), a low-pass filter suppresses out-of-channel interferers, allowing A_1 to be a non-
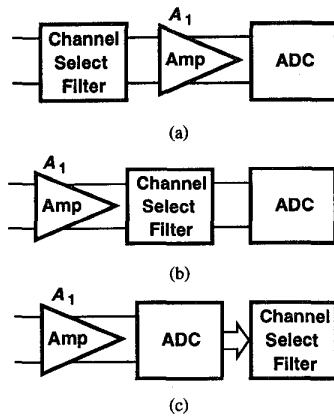

Fig. 16. Permutations of filtering, amplification, and digitization.

linear, high-gain amplifier and the ADC to have a moderate dynamic range (roughly 4 to 8 bits depending on the gain control in the RF domain and the type of modulation.) However, the noise-linearity-power trade-offs in the low-pass filter become problematic.

The second permutation, shown in Figure 16(b), relaxes the LPF noise requirements while demanding a higher performance of the amplifier. A typical one-stage differential amplifier may be utilized here to provide a gain of 20 dB before channel filtering. Furthermore, another amplifier may be interposed between the LPF and the ADC to overcome the noise of the latter.

The third permutation, Figure 16(c), suggests the possibility of channel filtering in the digital domain. In this case, the ADC must both achieve a high linearity so as to digitize the signal with minimal intermodulation of interferers and exhibit a thermal and quantization noise floor well below the signal level, which is in the range of a few hundred microvolts.

C. Frequency Synthesizers

The design of RF synthesizers, especially in CMOS technology, remains a challenging task. Issues related to synthesizer architectures, oscillators, and frequency dividers are described in [16, 17, 18, 19]. Germaine to CMOS implementations are the following difficulties: upconversion of flicker noise, trade-off between tuning range and phase noise, and high power dissipation in prescalers. We briefly review oscillators and quadrature generation techniques here.

Fig. 17(a) shows a Colpitts oscillator, where the voltage divider consisting of C_1 and C_2 transforms the resistance seen
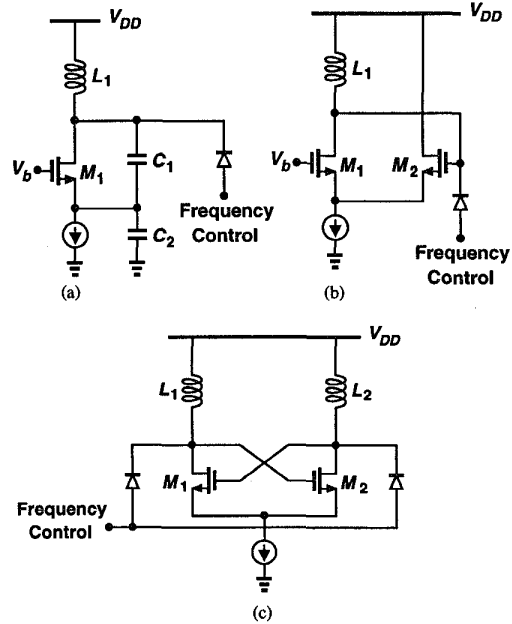

Fig. 17. (a) Colpitts oscillator, (b) use of source follower for impedance transformation, (c) differential negative-G_m oscillator.

looking into the source of M_1 [$\approx 1/(g_{m1} + g_{mb1})$] to a higher value, thereby minimizing resistive loading of the tank. As shown in Fig. 17(b), this transformation can alternatively be performed by means of a source follower, leading to a negative-G_m oscillator. With on-chip inductors, a fully differential configuration [Fig. 17(c)] proves extremely useful in driving mixers and single-sideband modulators.

Utilizing only one active device, the Colpitts oscillator exhibits a potentially lower phase noise, but it may fail to oscillate if the Q of the tank is low or the capacitance at the drain is large. This is because the circuit employs only one stage of gain. By contrast, the oscillator of Fig. 17(c) incorporates two stages of voltage gain, thereby operating reliably even with Q's as low as 3. It is also interesting (and alarming) to note that, in short-channel MOS technologies, the output impedance of the transistors becomes comparable with the equivalent parallel resistance of the tank, ultimately limiting the Q even if high-quality inductors and varactors are used.

A difficult operation commonly required in receivers is quadrature signal generation. A simple quadrature technique is to shift the signal by $\pm 45°$ using an RC-CR network (Fig.

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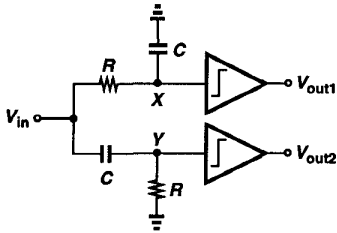18). Here, the phase difference between V_X and V_Y is 90°

Fig. 18. Quadrature network with limiters.

for all frequencies, but the output amplitudes are equal only at $\omega = 1/(RC)$. Thus, if the absolute value of RC varies with temperature and process, so does the frequency at which equal-amplitude quadrature signals exist. In the LO path, where the information lies in only the zero-crossing points, the amplitudes can be equalized by means of "limiting" stages, e.g., differential pairs. Amplitude limiting nevertheless becomes difficult in gigahertz circuits unless several stages are placed in cascade, at the cost of higher power consumption and larger mismatches between the two paths.

In addition, limiting stages entail "AM-to-PM conversion." In general, a nonlinear circuit with finite bandwidth exhibits a delay that depends on the input slew rate. Consider the simple circuit depicted in Fig. 19, where the capacitors represent
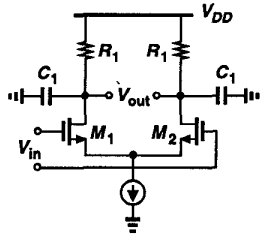

Fig. 19. Simple limiter.

the limited bandwidth. For a small-amplitude sinusoid with frequency ω applied at the input, the output differential current is also close to a sinusoid, thus experiencing a phase shift equal to $|\theta_1| = \tan^{-1}(R_1C_1\omega)$. If the input is a sinusoid with a large amplitude such that M_1 and M_2 rapidly switch at each zero crossing of V_{in}, the differential output current is close to a square wave, resulting in a delay equal to $R_1C_1 \ln 2$ and hence a phase shift equal to $|\theta_2| = R_1C_1\omega \ln 2$. In other words, the phase shift varies from $R_1C_1\omega \ln 2$ to $\tan^{-1}(R_1C_1\omega)$ according to the slew rate of the input. The key point is that a difference in amplitudes translates to a phase imbalance if the limiting stages do not provide adequate bandwidth.

IV. DESIGN EXAMPLES

In this section, we study three RF CMOS receivers designed for wireless applications so as to obtain a better view of the *system* performance that can be achieved.

A. 900-MHz ISM Band Receiver

Fig. 20 shows a direct-conversion receiver designed in 1-μm CMOS technology for operation in the 900-MHz ISM
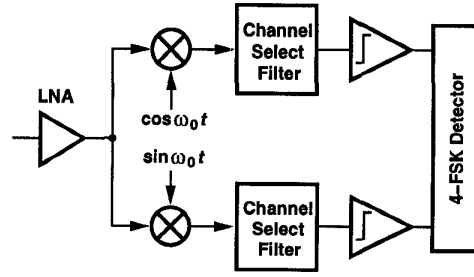

Fig. 20. ISM band receiver [9].

band [9]. Incorporating a differential common-gate LNA and grounded-source mixers, the circuit performs channel selection by means of a cascade of a second-order Butterworth filter and a sixth-order elliptic filter. The I and Q waveforms are then applied to limiters to amplify the levels, and subsequently to a 4-FSK detector. With an overall noise figure of 8.5 dB and IP_3 of -8.3 dBm, the receiver consumes approximately 150 mW from a 3-V supply.

B. DECT Receiver

Fig. 21 shows a 1.9-GHz dual-conversion receiver implemented in 0.6-μm CMOS technology for DECT applications
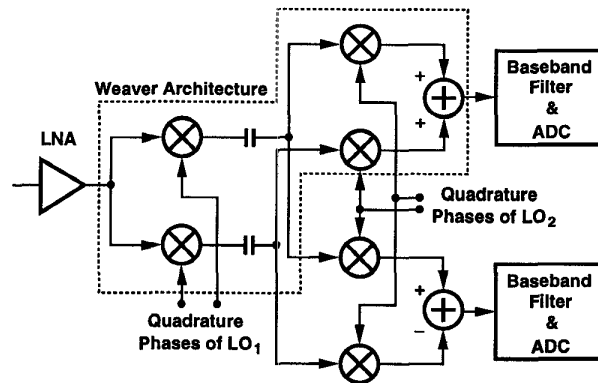

Fig. 21. DECT receiver [11].

[11]. Based on the Weaver architecture, the circuit consists of a differential front-end LNA, a quadrature downconversion to an IF of approximately 200 MHz, a second downconversion to zero frequency, and baseband channel selection and A/D conversion. In this architecture, the first LO has a fixed frequency while the second selects the desired channel. Thus, the close-in phase noise of the first LO can be suppressed by employing a wide loop bandwidth in its associated synthesizer.

The receiver baseband processing consists of a second-order Sallen and Key anti-aliasing filter, an eighth-order channel-select filter, and a 10-bit ADC. In addition, to cancel dc offsets due to self-mixing of the second LO, two externally-controllable current-steering digital-to-analog converters are used. The receiver achieves a sensitivity of -90 dBm with an input IP_3 of -7 dBm while consuming approximately 200 mW from a 3.3-V supply.

20.1.7

C. Dual-Band Receiver

Fig. 22 depicts a 900-MHz/1.8-GHz receiver designed in 0.6-μm CMOS technology for dual-band GSM/DCS1800 ap-
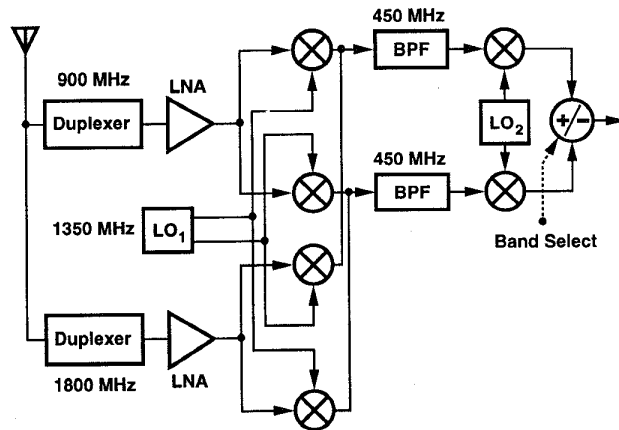

Fig. 22. Dual-band receiver [13].

plications [13]. Based on the Weaver architecture, the circuit exploits the fact that if the final outputs (after two quadrature downconversions) are added, the signal is obtained and the image is suppressed, and if they are subtracted, the reverse occurs. In other words, addition or subtraction of the outputs can select or reject two bands symmetrically located around the first LO frequency.

In the receiver of Fig. 22, the first LO frequency is set midway between the GSM and DCS1800 bands, making the two bands images of each other. Band selection is performed by enabling the corresponding LNA and RF mixers and adding or subtracting the outputs of the IF mixers. While the Weaver topology by itself does not provide adequate image rejection, the 900-MHz spacing between the signal and the image allows substantial image filtering in the front-end duplexers.

The dual-band receiver achieves an overall noise figure of 4.7 dB and IP_3 of -8 dBm at 900 MHz and 4.9 dB and -6 dBm at 1.8 GHz. The power dissipation is 75 mW from a 3-V supply.

V. WHAT NEXT?

CMOS technology must still resolve a number of practical problems in RF design.

• The variation of device and circuit parameters may substantially degrade the performance at the extremes of process and temperature conditions. Typical tracking and cancellation techniques used in analog systems are not easily applicable to circuits whose performance heavily depends on parasitics.

• Substrate coupling of signals that differ in amplitude by 100 dB is an important concern. Interestingly, spurs coupled through the substrate may not affect narrowband noise figure measurements, but, upon mixing with input interferers, may still corrupt the downconverted signal.

• Present MOS device models appear quite inadequate for RF circuit simulations. Negative capacitances, discontinuous derivatives, and incorrect noise representation are among the unsolved issues.

• At present, RF CMOS solutions consume significantly higher power than their bipolar or BiCMOS counterparts, perhaps because the principal thrust thus far has been to prove the *feasibility* of RF CMOS circuits. Architecture and circuit innovations along with device scaling may overcome this problem.

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