

# RF IC Design Challenges

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## Abstract

**This paper describes the challenges in designing RF integrated circuits for wireless transceiver applications. Receiver architectures such as heterodyne, homodyne, and image-reject topologies are presented and two transmitter architectures, namely, one-step and two-step configurations are studied. The design of building blocks such as low-noise amplifiers, mixers, and oscillators is also considered.**

## I. INTRODUCTION

The number of cellular telephone users in the United States exceeded 50 million in June 1997, only 14 years after the introduction of this product. By contrast, the wired telephone took 77 years and the television 24 years to reach such market penetration. It is also believed that about 20% of the world's population has never made a phone call . . .

The radio frequency (RF) and wireless market has suddenly expanded to unimaginable dimensions. Devices such as pagers, cellular and cordless phones, cable modems, and RF identification tags are rapidly penetrating all aspects of our lives, evolving from luxury items to indispensable tools. Semiconductor and system companies, small and large, analog and digital, have seen the statistics and are striving to capture their own market share by developing various RF products.

In addition to the market "push," the RF industry has also experienced a "pull" by the integrated circuits technology. Advances in silicon and GaAs devices continue to increase the level of integration and decrease the cost of RF circuits, allowing wireless products to compete with even their wired counterparts.

This paper describes the challenges posed to RF IC designers at the architecture and circuit levels. We first consider transceiver architectures such as heterodyne, homodyne, and image-reject receivers and one-step and two-step transmitters. Next, we study the design of various building blocks to understand the issues and trade-offs at the circuit level.

## II. TRANSCEIVER ARCHITECTURES

Complexity, cost, power dissipation, and the number of external components have been the primary criteria in selecting

receiver architectures. As IC technologies evolve, however, the relative importance of each of these criteria changes, allowing approaches that once seemed impractical to return as plausible solutions. Since filter requirements prohibit channel selection at RF, receivers first translate the input spectrum to a much lower frequency.

### A. Heterodyne Receivers

Heterodyne receivers downconvert the input to an "intermediate frequency" (IF), perform band-pass filtering and amplification, and translate the spectrum to a lower frequency again (Fig.1). In the case of phase or frequency modulation,

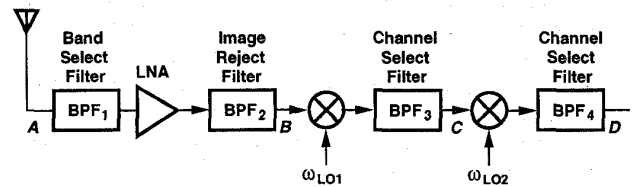


Fig. 1. Dual-conversion heterodyne receiver.

downconversion to the baseband requires both in-phase (I) and quadrature (Q) components of the signal. This is because the two sidebands of such signals carry different information and must be separated into quadrature phases in translation to zero frequency.

Perhaps the most important feature of the heterodyne receiver is its selectivity, i.e., the capability to process and select small signals in the presence of strong interferers. While selecting a 30-kHz channel at a center frequency of 900 MHz requires prohibitively large Q's, in Fig. 1 band-pass filtering is performed at progressively lower center frequencies.

Heterodyning nonetheless entails a number of drawbacks. The trade-off between image rejection and channel selection typically requires a relatively high IF, making it difficult to integrate the IF filter monolithically. Furthermore, the image-reject filter is a passive, bulky device that must be placed off-chip and driven as a 50-Ω load. This intensifies the trade-offs in the design of the low-noise amplifier.

In heterodyne architectures, the choice of the noise figure (*NF*), the third intercept point (*IP*<sub>3</sub>), and the gain of each stage in the chain depends on those of the preceding and following stages, thereby demanding considerable iteration at the architecture and circuit levels to arrive at an acceptable distribution of gain in the receiver building blocks. Moreover, each mixer generates many spurious components whose frequencies are related to those of the RF and IF signals and the oscillators. Some of these components may fall in the desired channel, degrading the signal quality. Thus, the "frequency

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planning” of the receiver directly impacts the performance of the receiver in the presence of interferers.

### B. Direct-Conversion Receivers

Direct-conversion (homodyne) receivers translate the channel of interest directly to zero frequency (Fig. 2). For frequency- and phase-modulated signals, the downconversion must provide quadrature outputs so as to avoid loss of infor-

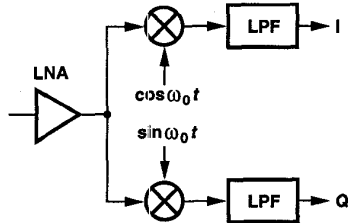


Fig. 2. Direct-conversion receiver.

mation.

Direct conversion offers two important advantages over a heterodyne counterpart. First, the problem of image is circumvented because  $\omega_{IF} = 0$ . As a result, no image filter is required and the LNA need not drive a 50- $\Omega$  load. Second, the IF filter and subsequent downconversion stages are replaced with low-pass filters and baseband amplifiers that are amenable to monolithic integration.

The simplicity of direct conversion nevertheless comes with a number of design issues. First, dc offsets due to mixing of the local oscillator (LO) leakage with itself corrupt the baseband signal and, more importantly, saturate the following gain stages [1, 2]. At the output of the mixer, such offsets can be as high as 10 mV whereas the signal may be as low as a few tens of microvolts. If the modulation scheme contains significant energy near dc, as is the case in most cellular and cordless phone standards, then ac coupling with practical values of capacitors and time constants severely degrades the signal. To remove dc offsets, periodic offset cancellation can be performed during idle times, but at the cost of  $kT/C$  noise [1].

Second, as depicted in Fig. 3, even-order distortion in the RF signal path generates low-frequency beats from large interferers. In the presence of mismatches and hence asymmetry in

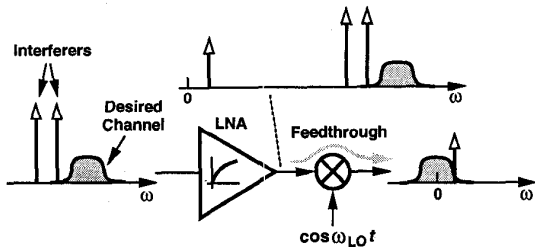


Fig. 3. Effect of second-order distortion in direct-conversion receivers.

the mixer, such components appear at the output, thus degrading the signal-to-noise ratio (SNR). This effect can be reduced by differential circuits or high-pass filtering the beats.

Owing to the limited gain provided by the LNA and the mixer, the downconverted signal is quite sensitive to noise.

Especially problematic here is the flicker noise of baseband amplifiers and filters in CMOS technology, making it desirable to realize a *high* gain in the RF and IF sections.

Another issue in direct-conversion receivers is the phase and gain mismatch introduced by the mixers. Phase mismatch gives rise to *cross-talk* between demodulated quadrature waveforms, lowering the SNR because the I and Q data streams are usually uncorrelated.

In addition to the above issues, the leakage of the LO signal to the antenna creates interference in the band of other users and must therefore be sufficiently small (typically between -60 and -80 dBm).

While most of these difficulties can be resolved by means of circuits techniques, the dc offset and flicker noise problems continue to challenge designers.

### C. Image-Reject Architectures

The issues related to the image-reject filter have motivated RF designers to seek other techniques of rejecting the image in a heterodyne receiver. One such technique originates from a single-sideband modulator introduced by Hartley [3]. Illustrated in Fig. 4, Hartley’s circuit mixes the RF input with the

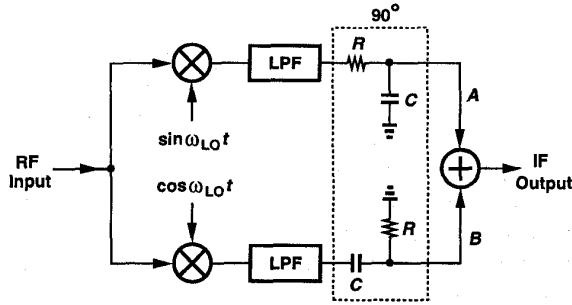


Fig. 4. Hartley image-reject receiver.

quadrature outputs of the local oscillator, low-pass filters and shifts the results by 90° before adding them together. It can be shown that the spectra at points A and B contain the desired band with the same polarity and the image with opposite polarity. The summed output is therefore free from the image.

The principal drawback of the Hartley architecture is its sensitivity to mismatches: with phase and gain imbalance, the image is only partially cancelled. Note that the effect of I/Q mismatch is much more severe here than in direct-conversion topologies. Also, the loss and noise of the shift-by-90° stage and the linearity of the adder are critical parameters. Furthermore, the variation of R and C introduces gain mismatch, limiting the image rejection ratio severely.

Shown in Fig. 5 is another image-reject architecture introduced by Weaver [4]. Replacing the 90° shift of Hartley’s circuit with a second quadrature mixing operation, this technique provides an arbitrary translation of the signal band without image interference. It can be shown that the subtraction of the spectrum at point C from that at point D produces the signal while suppressing the image.

The Weaver architecture is also sensitive to mismatches, but it avoids the use of an RC-CR network, thereby achiev-

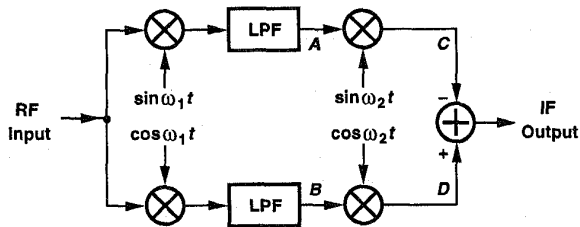


Fig. 5. Weaver image-reject receiver.

ing greater image rejection despite process and temperature variations.

#### D. Digital-IF Receivers

In the dual-conversion heterodyne architecture of Fig. 1, low-frequency operations such as the second set of mixing and filtering can be performed more efficiently in the digital domain. Shown in Fig. 6 is an example where the first IF signal

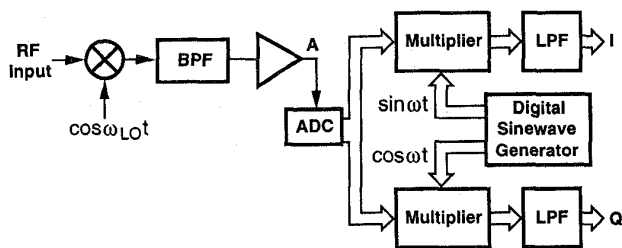


Fig. 6. Digital-IF receiver.

is digitized, “mixed” with the quadrature phases of a digital sinusoid, and low-pass filtered to yield the quadrature baseband signals. This approach is sometimes called a “digital-IF architecture.” Note that digital processing avoids the problem of I and Q mismatch.

The principal issue in this approach is the performance required of the A/D converter. Since the signal level at point A in Fig. 6 is typically no higher than a few hundred microvolts, the quantization and thermal noise of the ADC must not exceed a few tens of microvolts. Furthermore, if the first IF bandpass filter cannot adequately suppress adjacent interferers, the non-linearity of the ADC must be sufficiently small to minimize corruption of the signal by intermodulation. Additionally, the ADC must achieve an input bandwidth commensurate with the value of IF while consuming a reasonable amount of power.

The above requirements make it difficult to employ a Nyquist-rate ADC in the digital-IF architecture. Typical IF values of 50 to 200 MHz mandate sampling rates in the range of 100 to 400 MHz, and linearity, noise floor, and dynamic range requirements may necessitate resolutions greater than 14 bits. Such performance cannot be obtained in today’s A/D converters even if cost and power dissipation are not critical. The idea is nonetheless the subject of active research [5, 6].

#### E. One-Step Transmitters

If the transmitted carrier frequency is equal to the local oscillator frequency, the architecture is called a “one-step” topology. In this case, modulation and upconversion occur in

the same circuit. As shown in Fig. 7, the modulator is followed by a power amplifier and a matching network,<sup>1</sup> whose role is to provide maximum power transfer to the antenna and filter out-of-band components that result from the nonlinearities in the amplifier. Note that since the baseband signal is produced

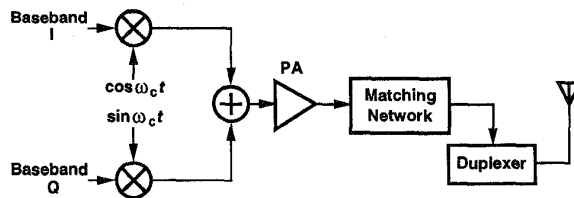


Fig. 7. One-step transmitter.

in the transmitter and hence is sufficiently strong, the noise of the mixers is much less critical here than in receivers.

The architecture of Fig. 7 suffers from an important drawback: disturbance of the transmit local oscillator by the power amplifier. Illustrated in Fig. 8, this issue arises because the PA output is a modulated waveform with high power and a

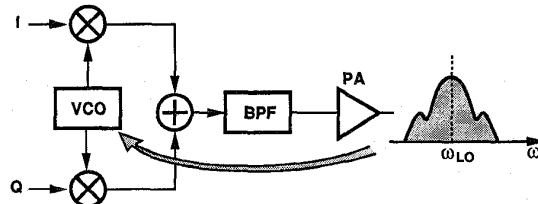


Fig. 8. Leakage of PA output to oscillator.

spectrum centered around the LO frequency. Despite various shielding techniques employed to isolate the VCO, the “noisy” output of the PA still corrupts the oscillator spectrum. This corruption occurs through a mechanism called “injection pulling” or “injection locking” [8]. The problem worsens if the PA is turned on and off periodically to save power.

The phenomenon of LO pulling is alleviated if the PA output spectrum is sufficiently higher or lower than the oscillator frequency. This can be accomplished by “offsetting” the LO frequency, i.e., by adding or subtracting the output frequency of another oscillator [9]. Fig. 9 shows an example where the output signals of VCO<sub>1</sub> and VCO<sub>2</sub> are mixed and the result is filtered such that the carrier frequency is equal to  $\omega_1 + \omega_2$ , far from either  $\omega_1$  or  $\omega_2$ .

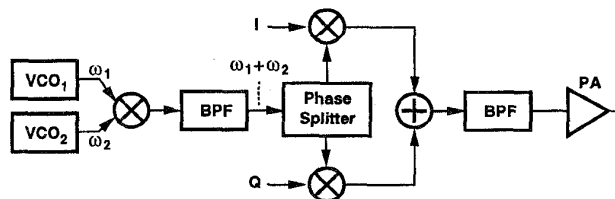


Fig. 9. One-step transmitter with offset LO.

<sup>1</sup>A band-pass filter may be interposed between the modulator and the PA to suppress the harmonics.

### F. Two-Step Transmitters

Another approach to circumventing the problem of LO pulling in transmitters is to upconvert the baseband signal in two (or more) steps so that the PA output spectrum is far from the frequency of the VCOs. As an example, consider the circuit shown in Fig. 10. Here, the baseband I and Q

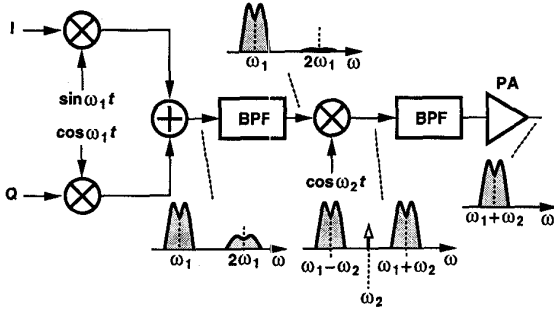


Fig. 10. Two-step transmitter.

channels undergo quadrature modulation at a lower frequency,  $\omega_1$ , (called the intermediate frequency) and the result is upconverted to  $\omega_1 + \omega_2$  by mixing and band-pass filtering. The first BPF suppresses the harmonics of the IF signal while the second removes the unwanted sideband centered around  $\omega_1 - \omega_2$ .

An advantage of two-step upconversion over the direct approach is that since quadrature modulation is performed at lower frequencies, I and Q matching is superior, leading to less cross-talk between the two bit streams. Also, a channel filter may be used at the first IF to limit the transmitted noise and spurs in adjacent channels.

The difficulty in two-step transmitters is that the bandpass filter following the second upconversion must reject the unwanted sideband by a large factor, typically 50 to 60 dB. This is because the simple upconversion mixing operation produces both the wanted and the unwanted sidebands with equal magnitudes. Owing to the higher center frequency, this filter is typically a passive, relatively expensive off-chip device.

## III. TRANSCEIVER CIRCUITS

The design of an RF transceiver heavily depends on the performance of its constituent subcircuits. Low-noise amplifiers, mixers, oscillators, frequency synthesizers, modulators, and power amplifiers are the principal RF building blocks in a typical system, each exhibiting trade-offs between noise, linearity, gain, power dissipation, frequency of operation, and supply voltage.

In this section, we present recent work in the design of some of these building blocks.

### A. Low-Noise Amplifiers and Mixers

As the first stages in the receive path, LNAs and mixers must process the signal with minimal noise and interference. In addition to the noise figure and third intercept point, the gain, port-to-port isolation, and power dissipation of these circuits impact the performance of a transceiver. The very

low noise required of LNAs usually mandates the use of only one active device at the input without any (high-frequency) resistive feedback. In order to provide sufficient gain while driving  $50\ \Omega$ , some LNAs employ more than one stage.

A bipolar LNA is shown in Fig. 11 [10], where the first stage utilizes a bond wire inductance  $L_e = 1.5\ \text{nH}$  to degen-

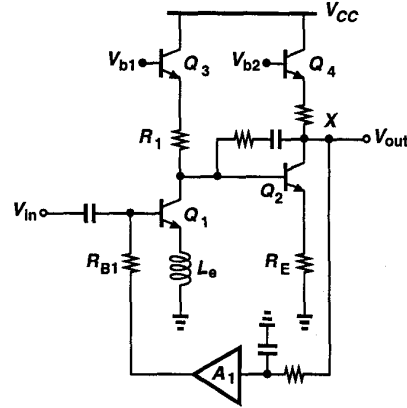


Fig. 11. LNA reported in [10].

erate the common-emitter amplifier,  $Q_1$ , without introducing additional noise. This technique both linearizes the LNA and makes it possible to achieve a  $50\text{-}\Omega$  input impedance. Bias voltages  $V_{b1}$  and  $V_{b2}$  and the low-frequency feedback amplifier  $A_1$  are chosen so as to stabilize the gain against temperature and supply variations. The resistive feedback in the second stage improves the linearity and lowers the output impedance. The circuit exhibits a noise figure of 2.2 dB, an  $IP_3$  of  $-10\ \text{dBm}$ , and a gain of 16 dB at 900 MHz.

Another bipolar LNA designed to drive a  $50\text{-}\Omega$  load is depicted in Fig. 12 [11]. Employing negative feedback through

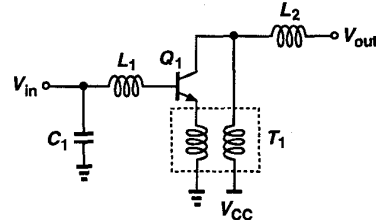


Fig. 12. LNA reported in [11].

a monolithic transformer to linearize the circuit, the LNA can operate with supply voltages as low as one  $V_{BE}$ . Interestingly, the transformer reduces the amplifier gain at both low and high frequencies, helping to stabilize the circuit. The external inductor  $L_1$  and capacitor  $C_1$  provide conjugate matching at the input.

Drawing 2 mA from a 1.9-V supply, the circuit of Fig. 12 achieves a noise figure of 2.8 dB and a gain of 9.6 dB at 1.9 GHz in an 11-GHz BiCMOS technology. The transformer feedback boosts the input  $IP_3$  to  $-3\ \text{dBm}$ .

A double-balanced bipolar mixer designed in conjunction with the above LNA is shown in Fig. 13 [11]. Here, an on-chip transformer both operates as a single-ended to differential converter and provides input matching. The bias current

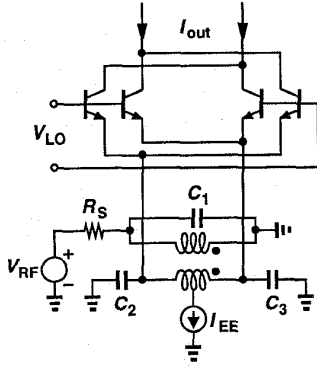


Fig. 13. Mixer reported in [11].

of the switching quad is established by  $I_{EE}$ , and capacitors  $C_1$ - $C_3$  effect resonance at the primary and secondary of the transformer.

A 1.9-GHz implementation of this configuration in an 11-GHz bipolar technology exhibits an NF of 10.9 dB with an  $IP_3$  of +2.3 dBm while dissipating 5 mW from a 1.9-V supply [11].

Shown in Fig. 14 is a 1.5-GHz CMOS LNA employing on-chip and off-chip inductors [12]. In a manner similar to that

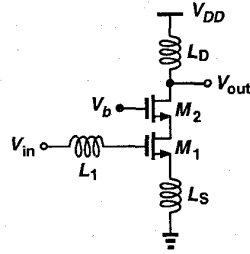


Fig. 14. LNA reported in [12].

described for the circuit of Fig. 11, this LNA incorporates  $L_S$  and  $L_1$  to create conjugate matching at the input. At 1.5 GHz, the on-chip inductor  $L_D$  provides significant voltage gain even though its  $Q$  is less than 4. By contrast, a load resistor would require a large voltage drop to provide a comparable gain.

The common-gate transistor,  $M_2$ , plays two important roles by increasing the reverse isolation of the LNA: (a) it lowers the LO leakage produced by the following mixer; (b) it improves the stability of the circuit by minimizing the feedback from the output to the input. Note that the same circuit with no cascode device would be prone to oscillation.

The LNA of Fig. 14 is followed by another cascode stage so as to drive a 50- $\Omega$  load, with each stage drawing 10 mA. Fabricated in a 0.6- $\mu\text{m}$  CMOS technology and operating from a 1.5-V supply, the circuit achieves a noise figure of 3 dB, a gain of 20 dB, and an input  $IP_3$  of -10 dBm.

Fig. 15 [13] shows the simplified circuits of an LNA and a mixer designed for a 900-MHz direct-conversion receiver. Requiring no image-reject filtering by virtue of the zero IF, the receiver allows direct cascading of the two circuits, obviating the need for a 50- $\Omega$  interface between the LNA and the mixer. The LNA is configured as a differential common-gate topol-

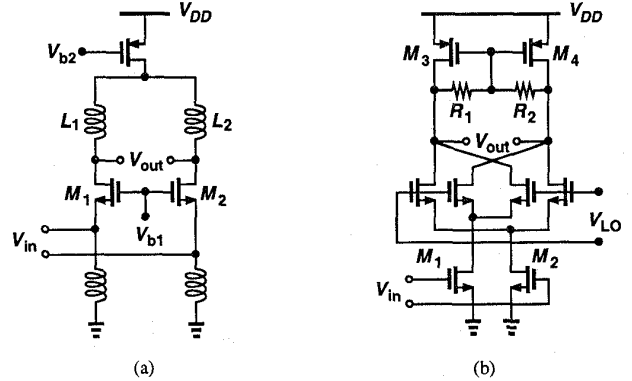


Fig. 15. (a) Common-gate CMOS LNA, (b) CMOS mixer with grounded-source input pair.

ogy, exhibiting an input impedance of 50  $\Omega$  (on each side) by proper sizing and biasing of  $M_1$  and  $M_2$ . However, since the transconductance of each transistor is roughly equal to  $1/(50 \Omega)$ , the noise figure cannot drop below a certain bound (2.2 dB with long-channel approximations).

The mixer resembles a Gilbert cell except that the sources of  $M_1$  and  $M_2$  are grounded. For square-law devices, this configuration does not produce third-order distortion whereas a differential pair biased at a constant tail current does. Thus, "grounded-source" MOS pairs potentially achieve a higher  $IP_3$  than do regular differential pairs. The load of the mixer consists of self-biased current sources  $M_3$  and  $M_4$  and gain-setting resistors  $R_1$  and  $R_2$ .

The LNA/mixer combination has been fabricated in a 1- $\mu\text{m}$  CMOS technology. Consuming 27 mW from a 3-V supply, the circuit exhibits an overall noise figure of 3.2 dB and an  $IP_3$  of +8 dBm.

## B. Oscillators

The local oscillators used to drive downconversion and upconversion mixers are embedded in a synthesizer loop to achieve a precise frequency definition. Phase noise, sidebands (spurs), tuning range, and settling behavior of synthesizers are critical parameters in RF applications, creating severe trade-offs as the number of external components is reduced.

Most integrated RF oscillators are configured as a negative- $G_m$  stage with inductive load. The idea is that an active circuit provides a negative resistance that cancels the finite loss in the inductors (and capacitors), thereby sustaining oscillation. While on-chip spiral inductors are attractive for higher levels of integration, various loss mechanisms limit the quality factor ( $Q$ ) to approximately 4 in typical CMOS technologies. As depicted in Fig. 16, wire resistance and electric and magnetic coupling to the substrate contribute loss. Another important issue, particularly in CMOS circuits, is the upconversion of  $1/f$  noise to the vicinity of the carrier frequency [14].

In bipolar technologies, spiral inductors exhibit slightly higher  $Q$ 's because the substrate is lightly-doped, i.e., electric and magnetic coupling of the inductor to the substrate is less pronounced. Fig. 17 shows a bipolar implementation

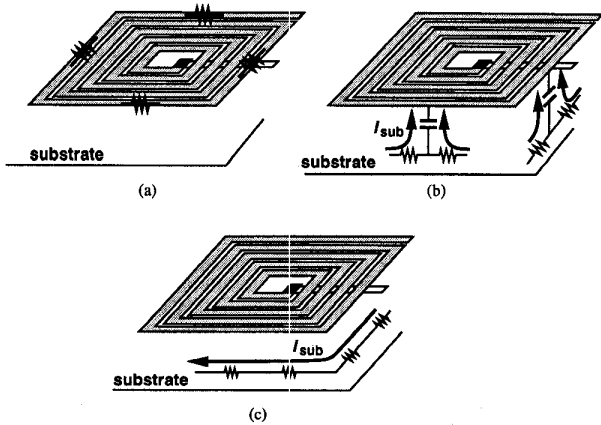


Fig. 16. Loss mechanisms in monolithic inductors.

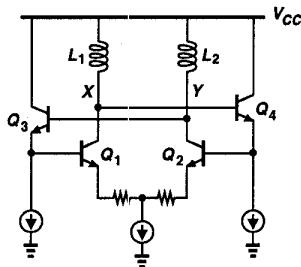


Fig. 17. Bipolar LC oscillator.

incorporating monolithic inductors with a  $Q$  of approximately 9 [15]. Using emitter followers in the loop to allow larger voltage swings at  $X$  and  $Y$ , the oscillator exhibits a phase noise of  $-105$  dBc/Hz at 100 kHz offset.

Fig. 18 shows a CMOS VCO topology designed for 900 MHz and 1.8 GHz [16]. Here, the transconductance ampli-

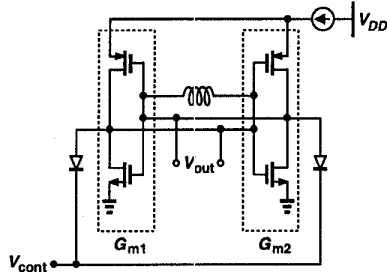


Fig. 18. CMOS negative- $G_m$  VCO.

fier incorporates both NMOS and PMOS devices to achieve a higher transconductance for a given bias current. However, the additional capacitance contributed by the PMOS transistors limits the tuning range further. Drawing approximately 10 mW from a 3-V supply, the 900-MHz version of the oscillator exhibits a phase noise of  $-108$  dBc/Hz at 100 kHz offset and a tuning range of 190 MHz [16].

An important issue in fully-monolithic LC oscillators is the trade-off between the phase noise and the tuning range [17]. For a given power dissipation, the relative phase noise decreases as the value of the tank inductance increases, but at the cost of making the capacitance of the transistors and the

inductor a significant part of the tank. As a result, the variable component of the tank capacitance drops. Also, at low supply voltages, the variation obtained from a varactor diode becomes more limited.

At present, oscillators used in demanding applications such as cellular telephones still incorporate external resonators (inductors, microstrip lines, or filters) to achieve an acceptably low phase noise and an adequate tuning range. Nonetheless, the properties of inductors built on silicon substrates are under vigorous study.

## REFERENCES

- [1] B. Razavi, "Design Considerations for Direct-Conversion Receivers," *IEEE Trans. Circuits and Systems, Part II*, vol. 44, pp. 428-435, June 1997.
- [2] A. A. Abidi, "Direct-Conversion Radio Transceivers for Digital Communications," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1399-1410, Dec. 1995.
- [3] R. Hartley, "Modulation System," US Patent 1,666,206, April 1928.
- [4] D. K. Weaver, "A Third Method of Generation and Detection of Single-Sideband Signals," *Proc. IRE*, vol. 44, pp. 1703-1705, Dec. 1956.
- [5] A. Hairapetian, "An 81 MHz IF Receiver in CMOS," *ISSCC Dig. Tech. Papers*, pp. 56-57, Feb. 1996.
- [6] S. Jantzi, K. Martin, and A. Sedra, "A Quadrature Bandpass  $\Sigma\Delta$  Modulator for Digital Radio," *ISSCC Dig. Tech. Papers*, pp. 126-127, Feb. 1997.
- [7] B. Razavi, *RF Microelectronics*, Upper Saddle River, NJ: Prentice Hall, 1998.
- [8] K. Kurokawa, "Injection Locking of Microwave Solid-State Oscillators," *Proc. IEEE*, vol. 61, pp. 1386-1410, Oct. 1973.
- [9] T. D. Stetzler et al, "A 2.7-4.5 V Single Chip GSM Transceiver RF Integrated Circuit," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1421-1429, Dec. 1995.
- [10] R. G. Meyer and W. D. Mack, "A 1-GHz BiCMOS RF front-end integrated circuit," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 350-355, March 1994.
- [11] J. R. Long and M. A. Copeland, "A 1.9GHz Low-Voltage Silicon Bipolar Receiver Front-End for Wireless Personal Communication Systems," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1438-1448, Dec. 1995.
- [12] D. K. Shaeffer and T. H. Lee, "A 1.5 V 1.5 GHz CMOS Low Noise Amplifier," *VLSI Circuits Symp. Dig. Tech. Papers*, pp. 32-33, June 1996.
- [13] A. Rofougaran et al, "A 1-GHz CMOS Front End IC for a Direct-Conversion Wireless Receiver," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 880-89, July 1996.
- [14] B. Razavi, "A Study of Phase Noise in CMOS Oscillators," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 331-343, March 1996.
- [15] B. Jansen, K. Negus, and D. Lee, "Silicon Bipolar VCOs for 1.1 to 2.2 GHz with Fully-Integrated Tank and Tuning Circuits," *ISSCC Dig. of Tech. Papers*, pp. pp. 392-393, Feb. 1997.
- [16] J. Craninckx, M. Steyaert, and H. Miyakawa, "A Fully Integrated Spiral LC CMOS VCO Set with Prescaler for GSM and DCS-1800 Systems," *Proc. CICC*, pp. 403-406, May 1997.
- [17] B. Razavi, "A 1.8 GHz CMOS Voltage-Controlled Oscillator," *ISSCC Dig. Tech. Papers*, pp. 388-389, Feb. 1997.