A 100-MHz 10-mW All-NPN Sample-and-Hold Circuit with 3-V Supply

Behzad Razavi
AT&T Bell Laboratories
Holmdel, NJ 07733, USA

Abstract—An all-npn open-loop sample-and-hold circuit employs capacitive coupling between input and output to allow differential voltage swings of 3 V in a 3.3-V system. Designed for use at the front end of analog-to-digital converters and fabricated in a 1.5-μm 12-GHz digital bipolar technology, the circuit exhibits harmonics 60 dB below the fundamental at a sampling rate of 100 MHz with a sinusoidal input of 10 MHz.

I. Introduction

Reduction of supply voltage to lower the power dissipation of digital circuits has created challenging tasks in analog and mixed-signal design. The loss of headroom and hence dynamic range has become more apparent in 3.3-V systems because the "turn-on" voltage of transistors has not scaled proportionally. In particular, despite their high transconductance, the unscalable base-emitter voltage of bipolar devices has made their use more difficult in low-voltage applications.

This paper introduces a low-voltage open-loop sample-and-hold technique that is compatible with all-npn bipolar technologies, achieving voltage swings of 3 V with a 3.3-V supply. The sample-and-hold amplifier (SHA) is intended for use at the front-end of multi-step analog-to-digital converters, where only the *held* values are processed by the following stages. Isolating the dc levels of the input and output stages by means of the sampling capacitor, the circuit exploits the high speed of bipolar transistors to achieve a sampling rate of 100 MHz while dissipating 10 mW.

II. Conventional Open-Loop SHAs

Owing to their fast switching, diode bridges have been popular in high speed sampling applications. Figure 1(a) depicts a typical sampling bridge along with minimum values of voltage drops whose sum determines the lowest supply voltage. It is seen that with a 3.3-V supply, the

circuit cannot accommodate input swings greater than a few hundred millivolts (if no Schottky diodes are available). Furthermore, the small bias voltage across R_1 yields large variations in the bridge current with common-mode level, thereby introducing substantial nonlinearity in the output signal.

Another all-npn SHA is shown in Figure 1(b) [1] in simplified form. It consists of a linearized unity-gain differential amplifier and emitter followers that are used as sampling switches. We note that this circuit, too, requires a minimum supply voltage of approximately 3.1 V. In practice, when designed for 10-bit linearity, this SHA topology allows a 1-V differential input swing with a 5-V supply [1].

III. Proposed SHA

A conceptual block diagram of the sample-and-hold circuit is shown in Figure 2. The SHA employs two channels in a quasi-differential architecture to improve the overall linearity, minimize the effect of common-mode pedestal and noise, and lower the droop rate. Each channel consists of an input buffer B_{in}, a sampling capacitor C_H, and an output buffer B_{out}. Switches S_1 and S_2 connect nodes M and N to fixed voltages V_{B1} and V_{B2}, respectively.

The circuit operates as follows. In the acquisition mode, S_1 is off and S_2 is on, holding node N at V_{B2}. Thus, if the offset and gain error of B_{in} are neglected, the voltage across C_H is equal to $V_{in} - V_{B2}$. In the transition to the hold mode, S_1 turns on, S_2 turns off, and V_M goes from V_{in} to V_{B1} (assuming B_{in} does not oppose this). Consequently, V_N changes from V_{B2} to $V_{B1} - V_{in} + V_{B2}$. The voltage held at node N is therefore equal to the input voltage at the sampling instant with opposite polarity plus a fixed shift $V_{B1} + V_{B2}$. This shift can be chosen so as to maximize both the input and output voltage swings.

An important concern in the architecture of Figure 2 is the nonlinearity caused by the total junction capacitance at node N, C_{jN}, when the circuit enters the hold mode. Since this node experiences the entire output swing, the voltage division between C_H and C_{jN} may introduce significant harmonic distortion in the held levels. While the quasi-differential architecture lowers this effect to some extent, C_H must nonetheless be sufficiently larger than C_{jN} to ensure linearities on the order of 10 bits.

The architecture of Figure 2 easily lends itself to an all-npn implementation. Figure 3 depicts the circuit for one of the channels. Here, emitter followers Q_1 and Q_4 function as B_{in} and B_{out}, respectively, and transistors Q_2 and Q_3 switch nodes M and N to proper voltages.

To illustrate the circuit's operation, we note that when CK is high, $V_P \approx -2$ V and hence Q_2 is off and Q_1 is on if V_{in} remains greater than V_P by a few hundred millivolts (Condition 1). At the same time, Q_3 establishes a voltage of approximately $-2V_{BE}$ at node N ($I_F R_2 \ll V_{BE}$). In the transition to the hold mode, CK goes low, V_P rises toward ground, bias current of Q_3 goes to zero, and its base voltage drops by approximately 300 mV. As V_M goes from $V_{in} - V_{BE}$ to $-V_{BE}$, V_N changes from $-2V_{BE}$ to $-V_{in} - 2V_{BE}$. Note that in this mode, Q_1 will be off so

long as V_{in} remains a few hundred millivolts below $V_P(=0)$ (Condition 2).

From the above observations we conclude that if $-1.7\ \text{V} \leq V_{in} \leq -0.2\ \text{V}$, then both Conditions 1 and 2 are satisfied and a voltage swing of 1.5 V (single-ended) is achieved. For $V_{in} = -1.7$ V, $V_N \approx +0.1$ V in the hold mode, slightly forward biasing the base-emitter junction of Q_4, but with negligible effect on speed.

A critical issue in all-npn SHAs is the input signal feedthrough during the hold mode, because junction capacitances of bipolar transistors can conduct appreciably even when devices are off. In the circuit of Figure 3, the feedthrough is suppressed by providing a low impedance $(g_{m2}^{-1} + R_1/(\beta+1))$ at node M during the hold mode, i.e., forming a high-pass filter for signals conducted by the base-emitter junction capacitance of Q_1. Simulations indicate that for a 1.5-V_{pp} 50-MHz sine input, the feedthrough is less than 1 mV. The bottom plate parasitic capacitance of C_H ($\approx 0.5C_H$) is placed at node M to further reduce the feedthrough.

IV. Experimental Results

The sample-and-hold circuit has been fabricated in a 1.5-μm 12-GHz digital bipolar technology [2]. The active area measures approximately 300 μm $\times$ 360 μm. The circuit has been tested on wafer using Cascade probes to provide the input and clock signals as well as power and ground connections. The output of each channel is sensed by a Tektronix SD14 FET probe (which has an input capacitance of 0.5 pF). The probes feed a Tek 11801B sampling oscilloscope capable of running FFT on the acquired waveform. All tests are performed with a 3-V supply.

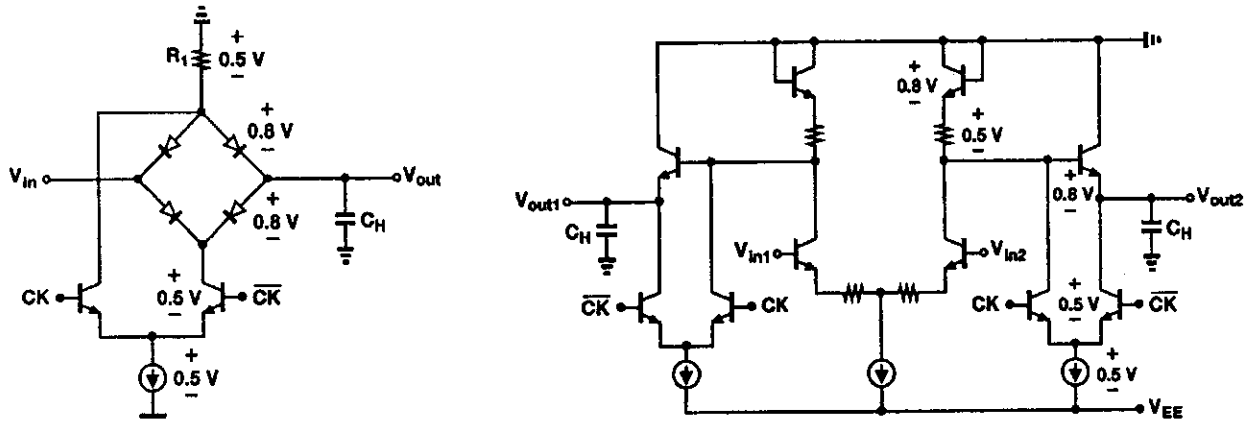
Shown in Figure 4 is the measured differential output of the SHA at a sampling rate of 100 MHz for an input sine of 10 MHz. The power dissipation of each channel is 5 mW. Subtracting one output from the other and calculating FFT of the resulting waveform, we obtain the spectrum shown in Figure 5, where the second and third harmonics are 60 dB below the fundamental. Note that the spectral purity is limited by the nonlinearity of the FET probes (hardly exceeding 60 dB). Furthermore, this measurement includes the nonlinear slewing when the circuit enters or leaves the hold mode. It is expected that if only the held values are considered, higher linearities can be attained [3].

References

[1] P. Vorenkamp and J. P. M. Verdaasdonk, "Fully bipolar, 120-Msample/s 10-b track-and-hold circuit," *IEEE J. Solid-State Circuits*, vol. SC-27, pp. 987-992, July 1992.

[2] K. G. Moerschel, *et al.*, "BEST: A BiCMOS-Compatible Super-Self-Aligned ECL Technology, " *Proceedings of CICC*, pp. 18.3.1-18.3.4, May 1990.

[3] K. Poulton, J. S. Kang, and J. J. Corcoran, "A 2 Gs/s HBT Sample and Hold," *Proceedings of IEEE GaAs IC Symp.*, pp. 199-202, 1988.



(a) (b)

Figure 1: Conventional SHAs, (a) diode bridge, (b) topology in [1].

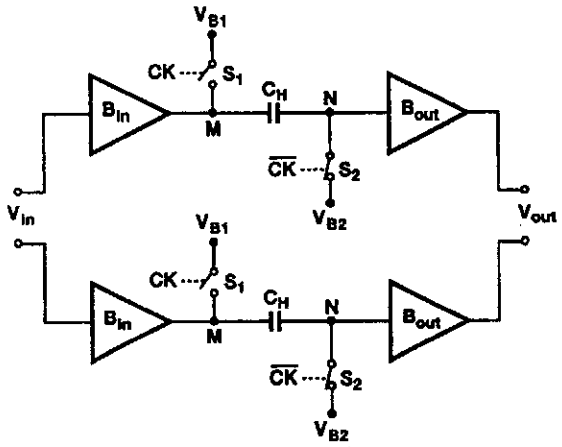


Figure 2: SHA block diagram.

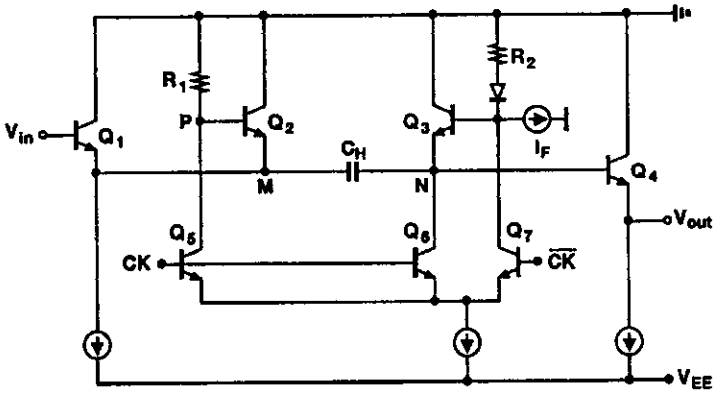


Figure 3: Implementation of one channel.

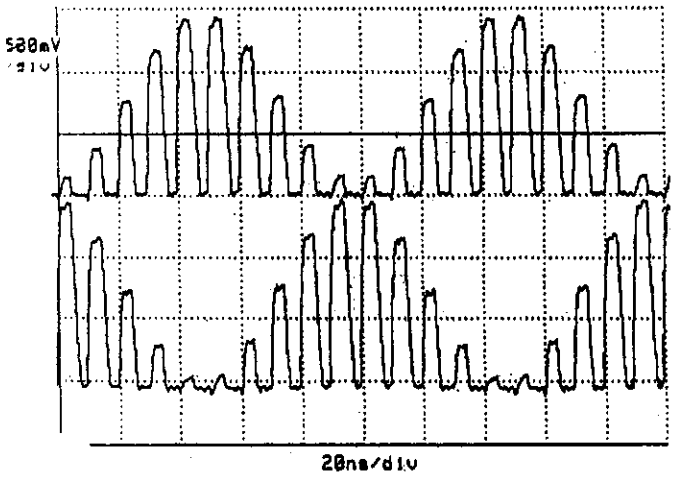


Figure 4: SHA measured output.

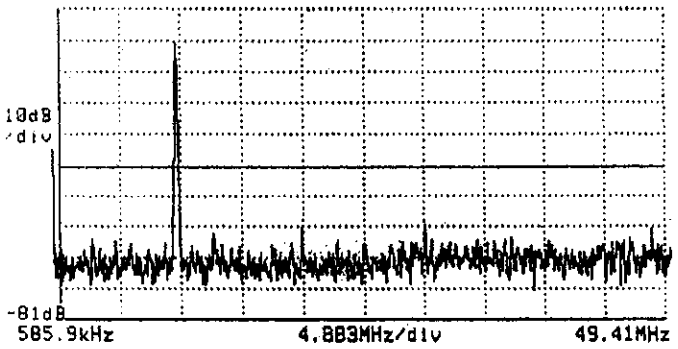


Figure 5: SHA measured output spectrum.