SP 23.6: A 1.8GHz CMOS Voltage-Controlled Oscillator

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This paper describes the factors that limit the tuning range of monolithic LC voltage-controlled oscillators (VCOs), especially at low supply voltages, and introduces circuit techniques that alleviate this problem. Incorporating such techniques, a 1.8GHz CMOS oscillator achieves a tuning range of 120MHz with a relatively constant gain while exhibiting a phase noise of -100dBc/Hz at 500kHz offset. The actual implementation is a quadrature generator consisting of two coupled oscillators [1]. Since the two oscillators are identical, only one is considered here.

A basic negative-G_m LC oscillator, with M_1 and M_2 canceling the loss in the two tanks is shown in Figure 1a. For a given frequency of oscillation, f_{osc}, and supply current, it is desirable to maximize the value of L_1 and L_2 to increase the voltage swings and hence decrease the *relative* phase noise. This is because the equivalent parallel resistance of an inductor can be expressed as $R_p \approx (L\omega)^2/R_S$, where R_S is the series resistance. Although L and R_S scale proportionally, R_p still increases linearly with L. The upper bound on the value of L_1 and L_2 is of course determined by their self-resonance frequency, f_{SR}.

Even if the inductors are designed so that $f_{SR} > f_{osc}$, their parasitic capacitance still constitutes a significant portion of the tank capacitance. For the 10nH inductors employed here, the contribution of C_1 and C_2 to nodes X and Y is approximately equal to 200fF. Furthermore, M_1 and M_2 must be sufficiently wide to ensure reliable oscillation (W/L=50µm/0.6µm), contributing another 160fF of gate capacitance to X and Y. Additionally, in the quadrature generator, each oscillator is loaded by both the input stage of the other oscillator and an output buffer - another 150fF of gate capacitance. Since with a 10nH inductor, the total capacitance must be in the vicinity of 780fF to allow oscillation at 1.8GHz, the variable part of the tank capacitance can only be about 270fF.

The tuning range is further limited if the supply voltage is reduced. Because the capacitance-voltage characteristic of pn-junction varactors is fundamentally unscalable, a narrower range of tuning voltage translates to a smaller relative change in the capacitance. More importantly, as the voltage swings become comparable with the reverse bias across the diode, the equivalent capacitance variation decreases, especially if the diodes must remain reverse-biased.

The tuning methods described in References 1and 2 either vary the bias current by a large factor or suffer from substantial variation in the gain of the VCO. In the oscillator of Figure 1(a), on the other hand, *IS1 provides* a constant bias current, and the common-mode voltage and hence the frequency are varied by adjusting the on-resistance of M_3. As V_{cont} increases, M_3 enters saturation, creating a sharp change in V_P and significant nonlinearity in the gain of the VCO. As depicted in Figure1(b), another transistor, M_4, driven by a down-shifted version of V_{cont} can be added such that as M_3 saturates, M_4 is still in the triode region, but with a higher on-resistance. In other words, M_3-M_5 provide a resistance from node P to V_{DD} that varies smoothly with V_{cont}. The voltage at P is ultimately clamped by M_6 to about 1.2V.

To further increase the tuning range, the anode voltage of D_1 and D_2 can be varied in the opposite direction with respect to their cathode voltage. Illustrated in Figure 1(c), the idea is to raise V_Q as V_P drops. Since $V_Q = V_{cont} - V_{GS5} - V_{GS7}$, M_5 and M_7 are sized and biased so that for V_{cont}=3.3V, V_Q=0.8V. Under this condition, D_1 and D_2 experience a forward bias of a few hundred millivolts but with no significant impact on the phase noise. Also, as I_{S1} enters the triode region, transistor M_8 maintains a relatively constant tail current for M_1 and M_2. Simulations indicate that the combination of these techniques doubles the tuning range of the oscillator.

Figure 1(d) shows the complete oscillator, including the differential pair M_9- M_{10} to sense the output of the other oscillator in the quadrature circuit. In this implementation, I_{S1}=2mA and I_{S2}=0.1mA.

The quadrature oscillator is fabricated in a digital 0.6µm CMOS technology. The varactor diodes, D_1 and D_2, are implemented as n-well-p^+ junctions, with the n-well strapped by n^+ rings to lower the series resistance (Figure 2(a)). Shown in Figure 2(b), each inductor consists of two stacked spiral structures, achieving roughly four times the inductance of one spiral of the same area. The hole in the middle is approximately 35µm wide. No special wafer processing steps are used.

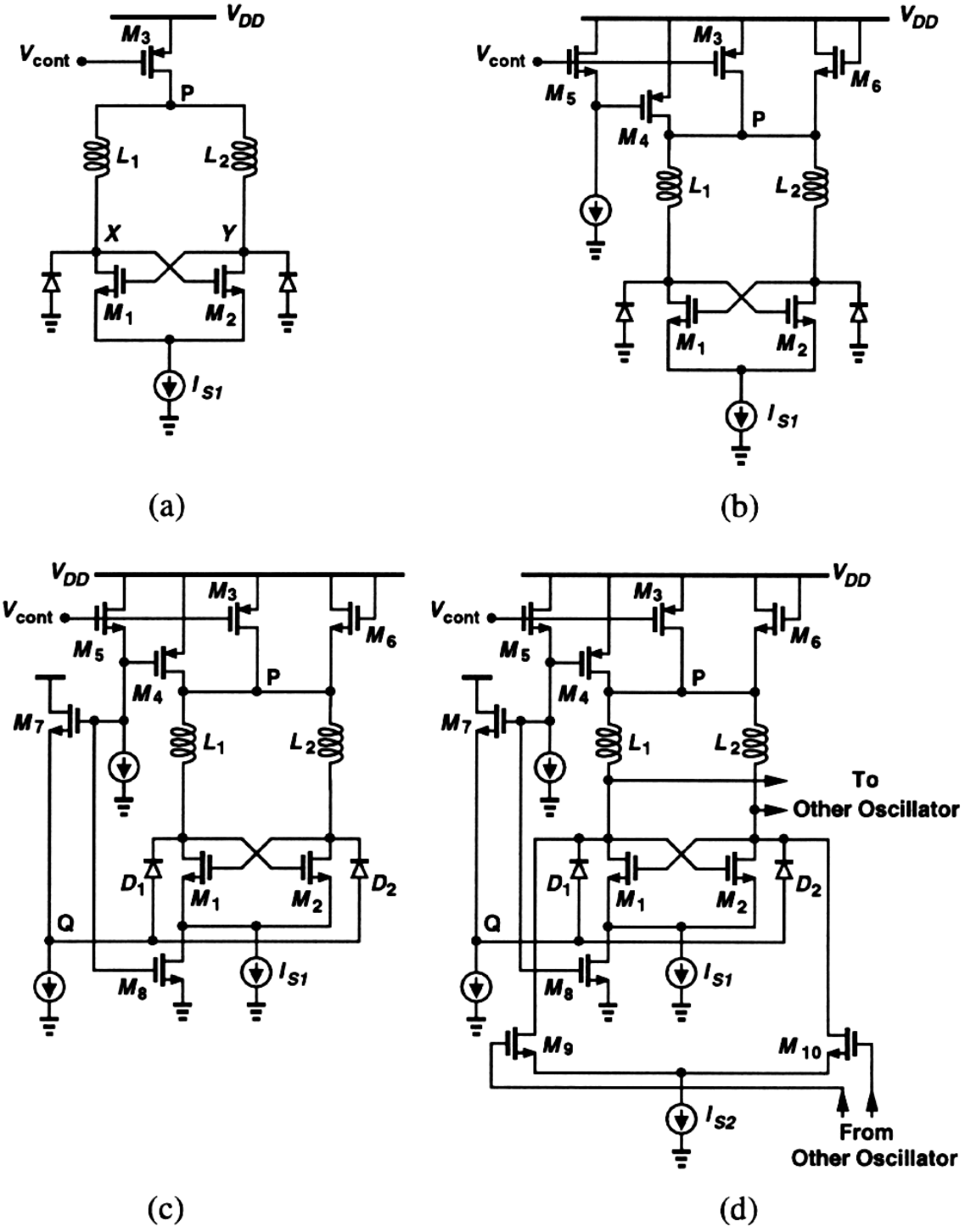
Figure 3 shows the output spectrum at 1.8GHz with a resolution bandwidth of 1kHz. The phase noise at 500kHz offset is -100dBc/Hz while each oscillator draws 2.3mA from a 3.3V supply.

Figure 4 shows the measured tuning characteristic of the VCO, indicating a frequency range of 120MHz and a gain of 114MHz/V. Table 1 summarizes VCO performance.

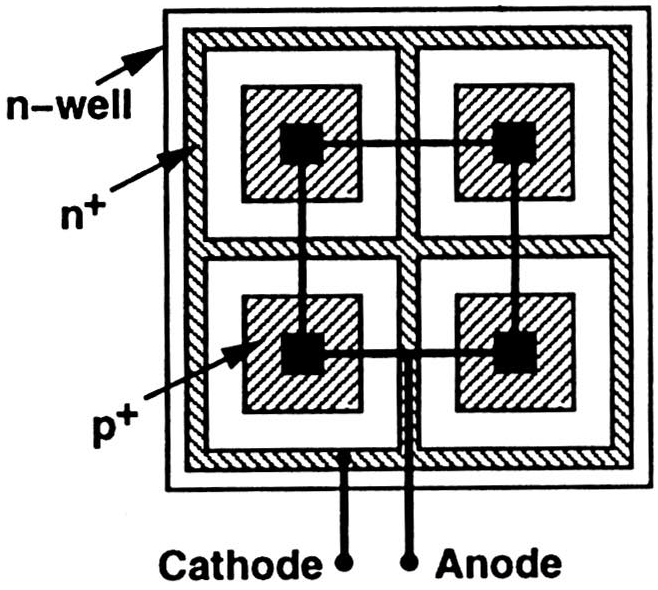
References:

[1] Rofougaran, A., et al, "A 900MHz CMOS LC Oscillator with Quadrature Outputs," ISSCC Digest of Technical Papers, pp. 392-393, Feb., 1996.

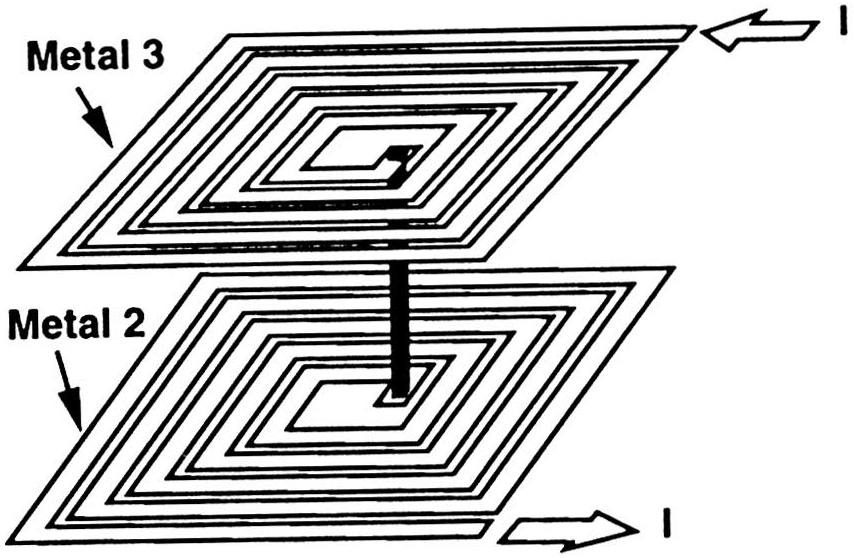
[2] Craninckx, J., M. Steyaert, "A 1.8 GHz Low-Phase Noise Spiral-LCCMOS VCO," VLSI Symp. Dig. Papers, pp. 30-31, June, 1996.



23-6-1: Evolution of VCO.

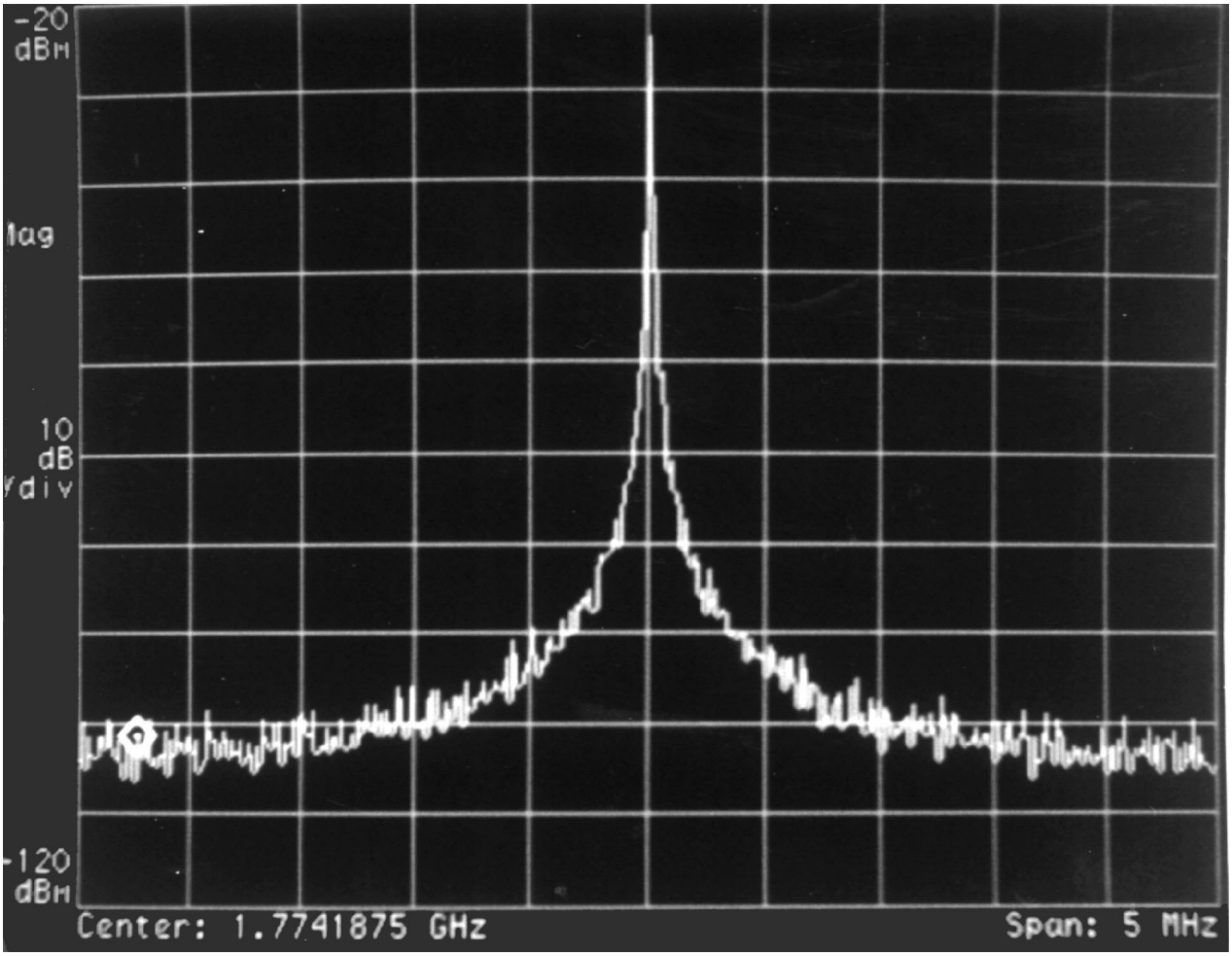


(a)

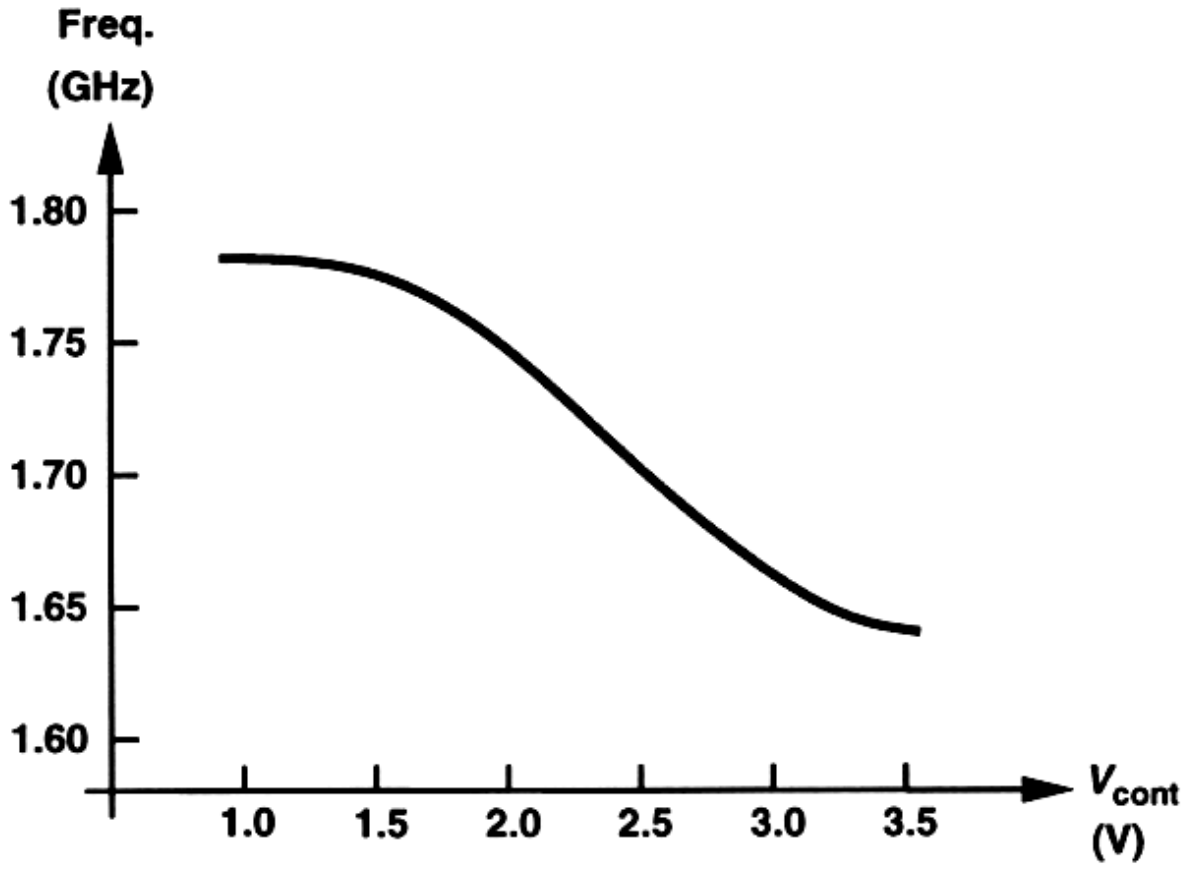


(b)

23-6-2: Implementation of (a) varactor diodes, (b) inductors.



23-6-3: Measured output spectrum (horiz. 500kHz/div., vert. 10dB/div.).



23-6-4: Measured tuning characteristic.

VCO frequency	1.8GHz
Tuning range	120MHz
Phase noise	-100dBc/Hz at 500kHz offset
Supply current	2.3mA/osc.
Supply voltage	3.3V
Technology	0.6µm CMOS

23-6-Table 1: Performance summary.