3.2

A 5.2-GHz CMOS Receiver with 62-dB Image Rejection

Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles

Abstract

A 5.2-GHz CMOS receiver employs a double downconversion heterodyne architecture with a local oscillator frequency of 2.6 GHz and applies offset cancellation to the baseband amplifiers. Placing the image around the zero frequency, the receiver achieves an image rejection of 62 dB with no external components while minimizing the flicker noise upconversion in the first mixing operation. Realized in a 0.25-μm digital CMOS technology, the circuit exhibits a noise figure of 6.4 dB, an IP_3 of -15 dBm, and a voltage conversion gain of 43 dB while draining 24 mW from a 2.5-V supply.

I. Introduction

As various wireless standards continue to populate the 2.4-GHz range, the next natural step is to extend the communications to the unlicensed 5-GHz band. In fact, the IEEE 802.11 committee has recently supplemented its 2.4-GHz standard with a 5-GHz version [1]. Additionally, the High Performance Radio Local Area Network (HIPERLAN) standard has been defined for operation in this band. With data rates as high as 54 Mb/s [1], these standards offer attractive solutions for data-intensive applications.

This paper describes a 5.2-GHz CMOS receiver for the HIPERLAN standard. Designed in conjunction with the synthesizer reported in [2] and based on a dual-conversion heterodyne architecture, the receiver incorporates a frequency planning that both simplifies the design of the frequency synthesizer and achieves a high image rejection with no external components. Fabricated in a 0.25-μm digital CMOS technology, the receiver exhibits a noise figure of 6.4 dB, an image rejection ratio of 62 dB, and a voltage gain of 42 dB while consuming 24 mW from a 2.5-V supply. Most of the architecture and circuit concepts introduced here can be directly applied to other standards as well.

II. Receiver Architecture

The receiver architecture and frequency planning are heavily influenced by both HIPERLAN's requirements and the synthesizer design constraints. Table 1 summarizes the receiver specifications recommended by HIPERLAN [3]. The standard incorporates Gaussian minimum shift keying (GMSK) modulation with a channel bandwidth of 23.5 MHz and stipulates a receiver sensitivity of -70 dBm for a packet error rate of 1%. With typical GMSK demodulators, such an error rate is achieved with a signal-to-noise ratio (SNR) of about 12 dB, yielding a maximum allowable noise figure of 18.3 dB. However, three other sources of SNR degradation must be taken into account: (1) roughly 3 dB of loss in the preselect filter that is usually interposed between the antenna and the low-noise amplifier (LNA); (2) about 1 dB of degradation due to the flicker noise in the baseband section; (3) about 1 dB of degradation due to the intersymbol interference (ISI) resulting from offset cancellation in the baseband.

Modulation	GMSK
Frequency Range	5.15–5.3 GHz
Channel Bandwidth	23.5 MHz
Sensitivity	−70 dBm
Spurious Emission	
30 MHz–1 GHz	−57 dBm
1 GHz–26.5 GHz	−47 dBm

Table 1. HIPERLAN receiver requirements.

Figure 1 shows the receiver architecture. The circuit performs two downconversions, each using a 2.6-GHz local oscillator (LO) frequency. As a result, the signal center frequency is translated from 5.2 GHz to 2.6 GHz and subsequently to zero. Each baseband branch then amplifies the signal while suppressing the dc offset component.

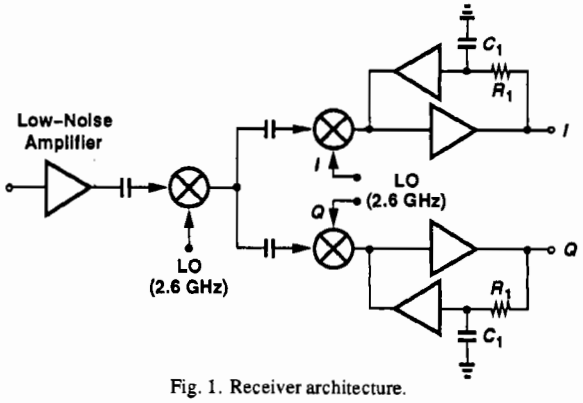

Fig. 1. Receiver architecture.

The frequency planning chosen in this work offers two advantages over that of conventional heterodyne or image-reject architectures. First, the frequency synthesizer operates at half the input frequency, thereby imposing less stringent requirements on its oscillator and frequency divider and achieving potentially more accurately-matched quadrature phases. Second, the image band is centered around the zero frequency,

 0-7803-6309-4/00/$10.00 © 2000 IEEE

thus experiencing a very high suppression by the antenna and the RF front end and obviating the need for an explicit image-reject filter.

The above architecture must nonetheless deal with three issues. First, since the image lies around the zero frequency, the flicker noise in the low-noise amplifier (LNA) and the input stage of the mixer is upconverted to the first IF, corrupting the signal (Fig. 2). Second, as the LO-IF feedthrough of

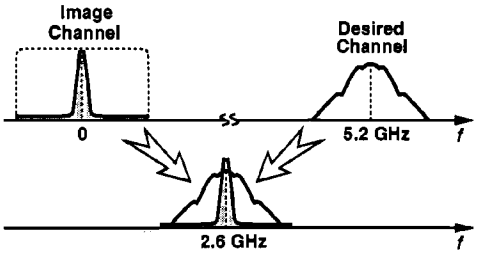

Fig. 2. Upconversion of flicker noise in the RF mixer.

the first mixer lies in the center of the IF band and cannot be filtered out, it may substantially desensitize the second downconversion mixers. Third, since no channel-selection filtering is performed at the first IF, the IF mixers must achieve even a higher linearity than the RF mixer. These issues are resolved in the design of the building blocks.

III. Building Blocks

Each of the four stages in the receiver chain, namely, the LNA, the RF mixer, the IF mixers, and the baseband amplifiers, directly impact the overall noise figure, linearity, gain, and power dissipation of the receiver. The circuit therefore requires both forward (LNA-to-baseband) and backward (baseband-to-LNA) design iterations.

The 0.25-μm digital CMOS technology used in this work provides five metal layers but no high-quality resistors and capacitors. Capacitors made of metal 3/metal 4/metal 5 sandwiches exhibit a relatively small bottom-plate capacitance ($\approx$ 15%) but suffer from a low density ($\approx$ 75 aF/μm^2). These considerations influence many of the receiver design choices.

A. RF Front End

While contributing noise and nonlinearity, the LNA and the RF mixer also determine the upconversion of flicker noise and the LO-IF feedthrough. To suppress the $1/f$ noise generated by the LNA, the amplified signal can be capacitively coupled to the input device of the mixer [Fig. 3(a)] but the $1/f$ noise of M_1 still falls in the image band. Thus, it is preferable to apply capacitive coupling between the mixer's input voltage-to-current (V/I) converter and the switching devices [Fig. 3(b)]. Here, the RF current produced by M_1 is absorbed primarily by M_2 and M_3, R_1 biases M_2 and M_3 while producing no flicker noise, and only a small fraction of the flicker noise of M_2 and M_3 is upconverted.

In Fig. 3(b), the V/I converter and the mixer draw twice as much supply current as the mixer of Fig. 3(a) does. Also, the dc compatibility of the LNA and the V/I converter is problematic. Both of these difficulties are resolved as shown in Fig. 4. The V/I converter, M_1, directly senses a level near V_{DD} and it is stacked on top of the mixer core, thus reusing

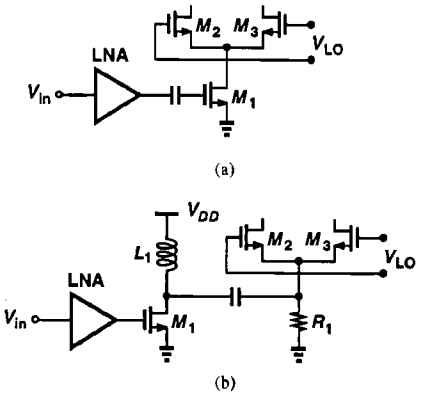

Fig. 3. Removal of flicker noise by capacitive coupling between (a) LNA and mixer, (b) V/I converter and mixer core.

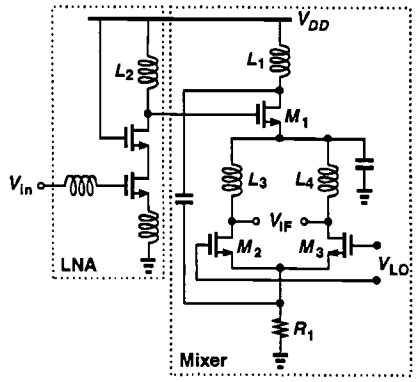

Fig. 4. Cascode LNA followed by stacked single-balanced mixer

the supply current. It is important to note that the stacking is possible here because the IF is sufficiently high to allow the use of inductors (rather than resistors) as the loads of the RF mixer. The bias current of the stack somewhat depends on the common-mode level of V_{LO}, but the impact on the overall receiver is negligible.

The single-balanced mixer topology of Fig. 4 produces excessive LO-IF feedthrough, desensitizing the IF mixers tremendously. It also makes the signal path more susceptible to the LO noise. The circuit is therefore modified to a double-balanced topology (Fig. 5), and the other input is connected to a dummy network (C_d, L_d, and M_d) to improve the symmetry. The second switching pair M_4-M_5 does inject additional noise to the output but the high gain of the LNA ($\approx$ 18 dB) lowers the contribution to the receiver noise figure. If means of converting the single-ended antenna signal to differential (e.g., external transformers) are available, then the LNA can be realized in differential form as well [5]. In such a design, the LNA would also drive the dummy network, reducing the overall noise figure slightly.

The resonant circuits used in the LNA and the RF mixer

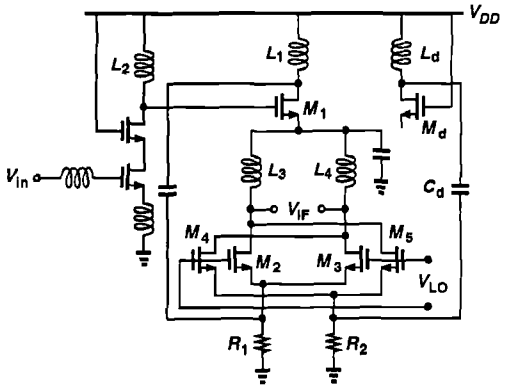

Fig. 5. Cascode LNA followed by stacked double-balanced mixer

must exhibit a high impedance in the band of interest so as to provide a large voltage gain. Since the quality factor of the inductors is relatively low, it is desirable to maximize the value of each inductor and/or minimize its parasitic capacitance. Figure 6(a) illustrates a typical two-layer inductor. It

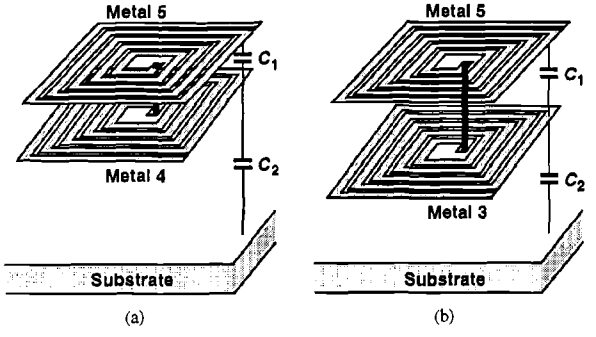

Fig. 6. Two-layer inductor made of (a) metal 5 and metal 4 layers, (b) metal 5 and metal 3 layers.

can be shown that the equivalent capacitance of this structure is equal to $(4C_1 + C_2)/12$ [4]. Thus, if C_1 is reduced, the self-resonance frequency f_{SR} rises substantially even if C_2 increases slightly. This observation leads to the structure depicted in Fig. 6(b), where the bottom spiral is moved away from the top one, reducing C_1 [4]. Applied to all of the inductors in the receiver, this modification increases the self-resonance frequency by 55%, allowing the use of 9-nH inductors in the 5-GHz signal path (L_1 and L_2) and 22-nH inductors at the 2.6-GHz IF (L_3 and L_4). Note that the modification does not change the total inductance or the substrate eddy currents significantly because the lateral dimensions are much greater than the vertical dimensions.

B. IF and Baseband Sections

Shown in Fig. 7, each of the quadrature IF mixers is realized as a double-balanced topology with grounded-source input transistors, achieving a third-intercept point (IP_3) of 1.26 V_{rms} (equivalent to +15 dBm in a 50-Ω system). The baseband signal is subsequently amplified by a differential PMOS stage designed for an IP_3 of 1.77 V_{rms} (equivalent to +18 dBm in a 50-Ω system). The high IP_3 required of the baseband

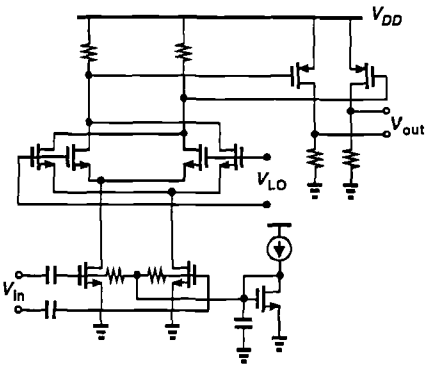

Fig. 7. IF mixer and baseband amplifier.

amplifier limits its voltage gain to approximately 15 dB with a 2.5-V supply. It also limits the IP_3 of the overall receiver.

The finite LO-IF feedthrough of the RF mixer and the self-mixing of the LO through the IF mixers create a large dc offset voltage, possibly saturating the baseband amplifier and other subsequent stages. As depicted in Fig. 8(a), the offset can be removed by capacitive coupling, but requiring large, relatively

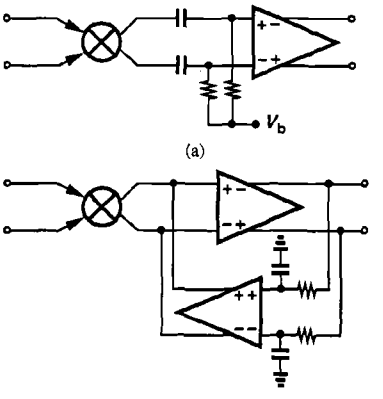

Fig. 8. Offset cancellation by (a) capacitive coupling, (b) negative feedback.

linear capacitors and large, low-capacitance resistors. Note that the parasitic capacitance of the resistors directly attenuates the signal. In the digital CMOS technology used here, linear capacitors can be implemented as a sandwich structure consisting of all metal layers and the polysilicon layer. The density, however, is only 200 aF/μm^2, translating to a very large area for the four capacitors necessary in the differential I and Q paths. By comparison, MOSFETs provide a density 30 times higher.

In this design, the offset is reduced by negative feedback around the baseband amplifier [Fig. 8(b)]. The critical advantage of this approach over that in Fig. 8(a) is that it employs only grounded capacitors and can therefore utilize MOSFETs. A 10-pF capacitor in this case consumes an area of 41 $\mu m \times 41$ μm whereas it would necessitate an area of 225 $\mu m \times 225$ μm if realized as a sandwich structure. Another advantage is that the parasitic capacitance of the resistors does not lower the gain at the frequencies of interest.

Offset cancellation introduces a notch in the spectrum of

0-7803-6309-4/00/$10.00 © 2000 IEEE

the downconverted signal, thereby creating intersymbol interference. For a GMSK signal, simulations indicate that if the corner frequency of the notch falls below roughly 0.1% of the bit rate, the resulting ISI impacts the bit error rate negligibly. With a bit rate of 23.5 Mb/s in HIPERLAN, the resistors in Fig. 8(a) must exceed 700 kΩ if each capacitor is limited to about 10 pF. The loop gain of the offset cancellation path in Fig. 8(b) further raises the minimum tolerable value to roughly 3 MΩ. Such a high value demands a very large area even if the resistors are made of n-well.

A long MOSFET with a well-defined gate-source overdrive voltage can act as a large floating resistor. Shown in Fig. 9(a) is a MOS device, M_1, operating in deep triode region

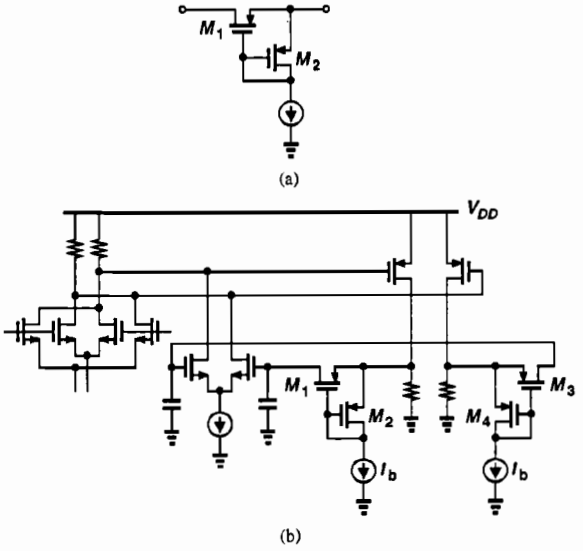

Fig. 9. (a) Floating resistor with controlled gate-source voltage, (b) offset cancellation in the baseband section.

with its gate-source voltage established by a diode-connected transistor, M_2. Here, R_{on1} tracks $1/g_{m2}$ if the overdrive voltage is large enough to overwhelm the threshold voltage mismatch between M_1 and M_2. The overall implementation of the dc feedback loop is illustrated in Fig. 9(b). With $(W/L)_{1,3} = 1\ \mu m/200\ \mu m$, $(W/L)_{2,4} = 1\ \mu m/10\ \mu m$, and $I_b \approx 1\ \mu A$, the corner frequency of the notch filter is on the order of a few kilohertz.

IV. Experimental Results

The receiver has been fabricated in a 0.25-μm CMOS technology and tested with a 2.5-V supply. Figure 10 shows a photograph of the die, which measures 600 μm×700 μm.

Table 2 summarizes the measured performance of the prototype. The image-rejection ratio (IRR) is evaluated by applying a 12-MHz input (the highest frequency in the image channel of Fig. 2) and measuring the downconverted baseband component. The rejection is limited to 62 dB by signal leakage through the substrate and the test board but, with another several tens of decibels of suppression provided by the antenna, the overall IRR is expected to reach 100 dB.

The offset cancellation loop reduces the output offset by about one order of magnitude. It is expected that subsequent stages would incorporate a similar technique to limit the offset. The measured corner frequency of the notch is equal to 1.5 kHz.

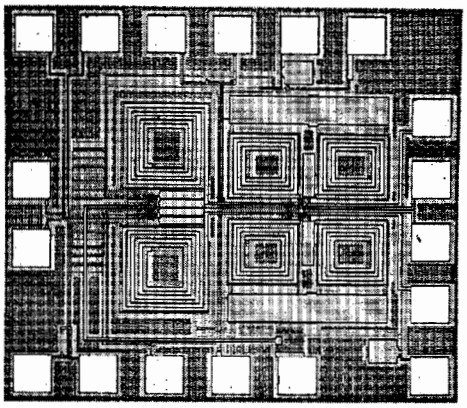

Fig. 10. Die photograph.

Center Frequency	5.2 GHz
Noise Figure	6.4 dB
Input IP_3	−15 dBm
1-dB Compression Point	−26.5 dBm
Image Rejection	62 dB
Voltage Gain	43 dB
LO Leakage to Antenna	
@ 5.2 GHz	−64 dBm
@ 2.6 GHz	−57 dBm
Output Offset Voltage	25 mV
Power Dissipation	24 mW
Supply Voltage	2.5 V
Technology	0.25−μm CMOS

Table 2. Receiver measured performance.

Both the LO frequency and its second harmonic (generated at the sources of M_1-M_4 in Fig. 5) leak to the RF input. The cascode LNA suppresses the 5.2-GHz leakage to −64 dBm. The 2.6-GHz leakage arises primarily from the traces on the board but it would be suppressed further by the selectivity of the antenna. Both leakage levels are well below the HIPERLAN limits (Table 1).

References

[1] A. Dutta-Roy, "Networks for Homes," *IEEE Spectrum*, pp. 26-33, vol. 36, Dec. 1999.

[2] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology," *VLSI Circuits Symp. Dig. of Tech. Papers*, pp. 117-120, June 1999.

[3] ETSI TC-RES, "Radio Equipment and Systems (RES); High Performance Radio Local Area Network (HIPERLAN); Functional Specification," ETSI, 06921 Sophia Antiplois Cedex, France, July 1995.

[4] A. Zolfaghari, A. Y. Chan, and B. Razavi, "Stacked Inductors and 1-to-2 Transformers in CMOS Technology," submitted to *IEEE Custom Integrated Circuits Conference*, 2000.

[5] H. Samavati, H. R. Rategh, and T. H. Lee, "A 12.5-mW CMOS Front End for a 5-GHz Wireless LAN Receiver," *VLSI Circuits Symp. Dig. of Tech. Papers*, pp. 87-90, June 1999.