A 2-GHz 1.6-mW Phase-Locked Loop

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High-speed low-power phase-locked loops (PLLs) are an integral part of frequency synthesizers and clock recovery circuits. This paper describes the design of a 2-GHz PLL that employs a number of circuit techniques to reduce the power dissipation to 1.6 mW with a 3-V supply. Fabricated in an 18-GHz 0.6-μm BiCMOS technology, the PLL utilizes fully-differential signals to improve the rejection of common-mode disturbances.

Figure 1 shows a block diagram of the PLL, a fairly standard architecture, but with the phase detector, the low-pass filter (LPF), and the voltage-controlled oscillator (VCO) merged so as to save power dissipation. The amplifier interposed between the LPF and the VCO operates at low frequencies, thus consuming negligible power. The PLL design is described in a progression starting with the VCO circuit.

The VCO can be implemented as a simple ring oscillator. While such topologies with three or even two stages have been used successfully [1-3], it is desirable to further reduce the number of stages so that power dissipation is minimized. We note that if the number of stages is lowered from two to one, the power dissipation corresponding to a given speed decreases by approximatley a factor of *four*. This is because if one stage is removed from a two-stage configuration oscillating at ω_0, the resulting circuit oscillates at approximately $2\omega_0$ while dissipating *half* the power. Thus, the power dissipation of the one-stage topology can be lowered by another factor of two so as to obtain an oscillation frequency of ω_0.

Shown in Figure 2(a) is a differential gain stage with negative feedback. This circuit fails to oscillate because the total phase shift around the loop at the unity-gain frequency of the amplifier does not reach 180°. To introduce additional phase shift, we add cross-coupled pairs Q_5-Q_6 and Q_7-Q_8 in the signal path [Figure 2(b)]. At a frequency of 2 GHz, the capacitance seen at nodes A-B and E-F appears as a moderate impedance to ground, providing substantial gain and phase shift around each local positive feedback loop. The circuit thus oscillates with nearly complete switching of the devices.

In the circuit of Figure 2(b), the collector currents of Q_3 and Q_4 experience considerable change because of the total capacitance seen at M-N and E-F. These currents can therefore be considered as the output of the VCO and mixed with the input signal as in a Gilbert cell [Figure 3(a)]. To avoid saturating Q_3 and Q_4, transistors Q_9 and Q_{10} shift the voltage swings at G and H down by one V_{BE}. Also, R_{B1} and R_{B2} provide inductive peaking at the emitters of Q_9 and Q_{10}, thereby boosting the gain at 2 GHz, allowing the use of smaller values for R_{C1} and R_{C2}, and relaxing the gain-speed-power trade-off.

The circuit of Figure 3(a) requires a supply voltage greater than $4V_{BE}$ because of the path comprising the base-emitter junctions of Q_9, Q_4, Q_8, and Q_1 (and a similar path through Q_{10}, Q_3, Q_7, and Q_2). To alleviate the voltage headroom limitation, the signal at nodes E and F can be coupled to the *emitters* of Q_1-Q_2, with a swap in the differential voltages to maintain negative feedback. This is illustrated in Figure 3(b). However, the base voltage of Q_1 and Q_2 must now be defined accurately to ensure proper bias current sharing with Q_7-Q_8. This difficulty is overcome in Figure 3(c), where the bases of Q_1 and Q_2 are driven by signals that have proper common-mode level and are opposite of those applied to the emitters of Q_1 and Q_2.

The final combination of the VCO/mixer/LPF is shown in Figure 4. Here, differential pairs Q_{11}-Q_{12} and Q_{13}-Q_{14} control the VCO output frequency by adjusting the turn-on delay of the cross-coupled pair Q_5-Q_6, and additional current sources I_1-I_4 increase the frequency of oscillation with negligible power penalty. Small NMOS devices ($W/L = 1.5\ \mu$m/$0.6\ \mu$m) with low parasitics prove especially useful in the implementation of these current sources. Note that the VCO output signal is taken from the collectors of Q_9-Q_{10} to minimize the effect of the input capacitance of the output buffer.

The LPF is realized as a lead-lag network at the output of the mixer (Figure 4). Amplifier A_1 in Figure 1 is simply a differential stage with proper level shift.

The PLL has been fabricated in an 18-GHz 0.6-μm BiCMOS technology, and tested on-wafer using high-speed Cascade probes. Operating from a 3-V supply, the circuit (excluding the output buffer) draws 530 μA. Shown in Figure 5 is the PLL output waveform at 2 GHz, exhibiting an rms jitter of approximatly 2.8 psec. The circuit achieves a tracking range of 110 MHz and a capture range of 70 MHz.

Figure 6 shows the output spectrum of the PLL. The upper left trace corresponds to the free-running VCO and the lower right trace to the locked circuit. The phase noise under locked conditions is equal to -110 dBc/Hz at 400 kHz offset.

References

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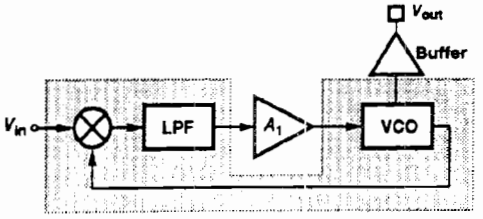

Fig. 1. PLL block diagram.

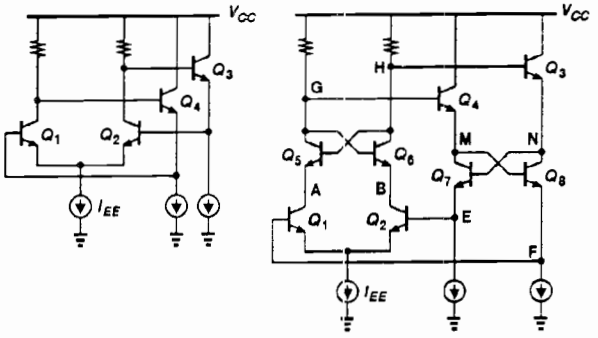

Fig. 2. (a) Simple gain stage with negative feedback, (b) basic VCO.

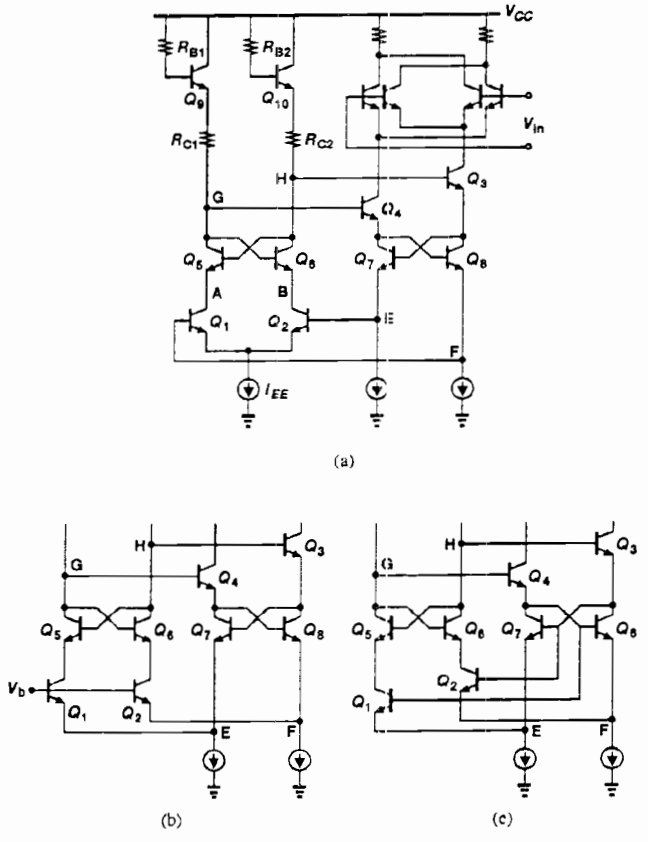

Fig. 3. (a) VCO with mixer, (b) coupling of feedback signal to emitters of Q_1 and Q_2, (c) modification of (b) to eliminate V_b.

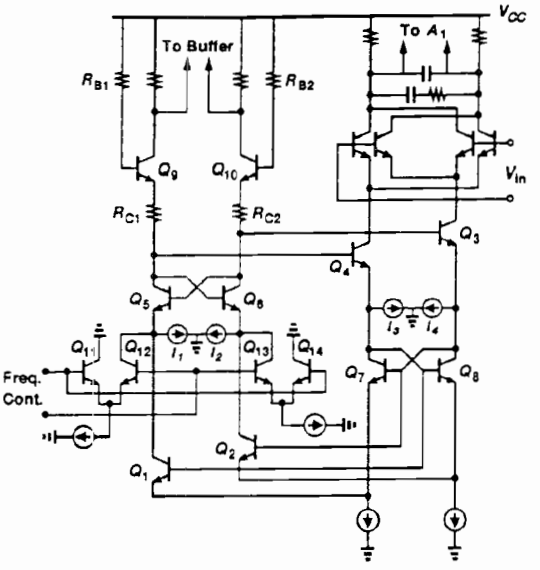

Fig. 4. VCO/mixer/LPF circuit.

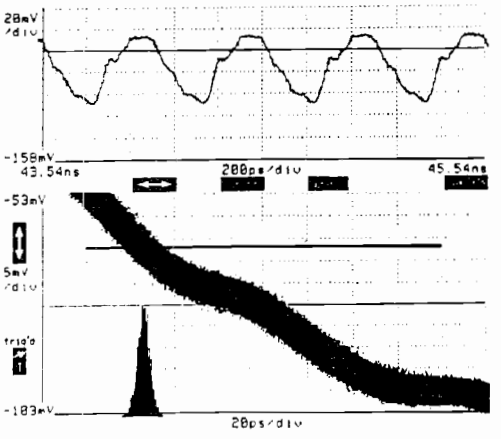

Fig. 5. PLL output waveform at 2 GHz.

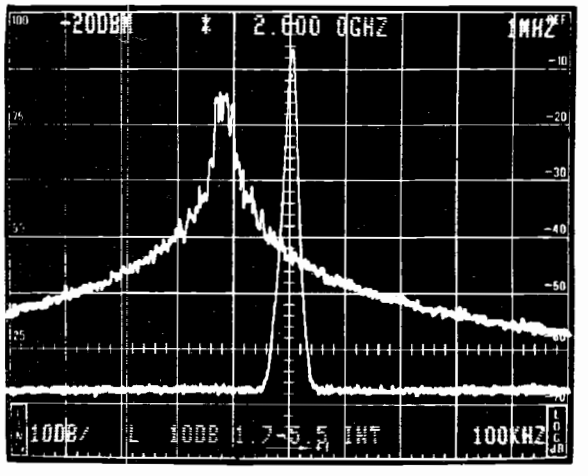

Fig. 6. PLL output spectrum at 2 GHz. (Horiz. 1 MHz/div., vert. 10 dB/div.)