A Receiver Architecture for Intra-Band Carrier Aggregation

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Abstract—A block downconversion receiver incorporates a digital image rejection technique to support multiple aggregated carriers by one receive path and one frequency synthesizer. A prototype consisting of a CMOS RF front end and an FPGA back end exhibits an image rejection ratio (IRR) of at least 70 dB across 2 GHz $\pm$ 25 MHz and reconstructs a -76-dBm 64-QAM signal with an EVM of -30 dB in the presence of another channel 40 dB higher.

Carrier aggregation is an attractive approach to increasing the bandwidth and hence the data rate in wireless communications. It is possible to place a single LO frequency mid-way between two carriers in a Weaver receiver so as to reconstruct simultaneously both signals [1]. However, this approach faces several issues: lack of frequency-dependent IRR calibration, the need for harmonic-rejection IF mixers, and the direct increase in analog complexity and power dissipation as the number of channels increases. The first issue is particularly important as even a 2% mismatch between the poles of two first-order I and Q analog filters limits the usable bandwidth to 10% of the pole frequency if IRR must exceed 60 dB.

This paper describes a "scalable" block downconversion receiver architecture that, by virtue of a background digital image calibration technique, can support multiple carriers while providing an IRR greater than 70 dB. A new broadband low-noise amplifier (LNA) is also introduced.

Receiver Architecture The receiver architecture is shown in Fig. 1 along with spectra for a four-carrier example. The LO frequency is placed mid-way between the outermost carriers, thereby downconverting the block to an IF of no more than 35 MHz [1]. The quadrature IF signals are low-pass filtered, digitized, and applied to an image rejection module before complex downconversion to baseband. Of course, the two ADCs must digitize the IF components along with downconverted in-band blockers. Among the in-band blocker profiles in [2], that containing a 5-MHz wide desired signal and a 40.5-dBc blocker demands the widest ADC dynamic range (DR). Since a 64-QAM constellation dictates an SNR of about 24 dB for an acceptable BER, we conclude that the ADC must achieve a minimum DR of 64.5 dB. Fortunately, recent work on ADCs has reported a 14-bit, 80-MHz converter that achieves an SNR of 71 dB and an SFDR of 80 dB at the Nyquist rate while consuming 31 mW [3]. If running at 80 MHz, this ADC oversamples the desired signal by a factor of 8, achieving a DR of roughly 71 dB $+10\log 8 \approx 80$ dB, providing ample margin for the above scenario.

Illustrated in Fig. 2, our proposed algorithm is based on two principles. (1) With analog gain and phase mismatches of ϵ and θ, respectively, we can simply multiply, in the frequency domain, the I component by a complex number $\alpha = (1+\epsilon)\cos\theta + j(1+\epsilon)\sin\theta$ so as to remove the mismatches. (2) If two overlapping channels at IF carry a power of P_A and P_B, then $|I|^2$, $|Q|^2$, and the inner product, $I{\cdot}Q$, yield the values shown in Fig. 2, from which we can derive $Re\{\alpha\}$ and $Im\{\alpha\}$. Remarkably, since $Im\{\alpha\}$ and $Re\{\alpha\}$ can be calculated for each FFT bin, the frequency-dependent mismatches are corrected with a fine frequency resolution.

The operations required in the mismatch estimator are performed by bit-serial arithmetic using only adders and registers [4] because the computation of α can be as slow as temperature- and supply-induced drifts in ϵ and θ. The phases of ω_{IF} in the downconverter are produced by numerically-controlled oscillators, i.e., an accumulator followed by a look-up table, yielding harmonic-free mixing. The downconverter in Fig. 2 is repeated according to the number of intra-band carriers.

Receiver Front End Fig. 3 shows the implementation of the front end, designed for the LTE range of 700 MHz to 2700 MHz. We propose a broadband LNA with active feedback so as to obtain a low noise figure (NF), acceptable input matching, and single-ended to differential conversion.

The circuit is designed such that, with the load presented by the mixers and the TIAs, the voltage gain of Inv_2 is about unity and $R_{in} = 50\,\Omega$. The LNA noise figure is 1.76 dB.

Operating with low supply voltages, this LNA stands in contract to the noise-cancelling topology in [5], which does *not* cancel the noise of the input CG device if it drives balanced mixers and TIAs (and employs unequal drain resistors).

In order to establish a well-defined bias current for the inverters in the LNA, a servo loop adjusts the PMOS body voltage of a replica inverter, Inv_{rep}, so as to force V_1 equal to V_2, thus driving the bias current of Inv_{rep} toward I_{REF1}. This method obviates the need for placing a bias current source in series with the source of the inverter transistors, allowing a greater voltage headroom and hence higher linearity.

Experimental Results The receiver front end in Fig. 1 has been fabricated in TSMC 45-nm digital CMOS technology and tested with off-the-shelf ADCs and an FPGA back end. Shown in Fig. 4, the active die area is $450\ \mu\text{m} \times 350\ \mu\text{m}$. Tested at 2 GHz, the prototype dissipates 15 mW.

Shown in Fig. 5, the measured NF varies from 3.65 dB to 3.85 dB, and the IRR exceeds 70 dB across the IF bandwidth. Figure 6 presents the measured performance for two carriers. As a first test, a tone is placed in Channel 1 and a modulated signal in Channel 2. We observe that the image of Channel 2 is reduced by more than 70 dB after α in Fig. 2 settles (in 1 ms) to its correct value. In the next test, a QPSK or 64-QAM signal resides in Channel 1 and another modulated signal 40 dB higher in Channel 2. The measured constellations in Fig.

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6 demonstrate that the image due to Channel 2 is greatly suppressed, yielding an EVM of −30 dB for the 64-QAM signal.

The complexity and power of the digital back end have been conservatively estimated from the FPGA implementation. The FFT and IFFT blocks, the mismatch estimator logic, and the downconverters require about 95k gates, which, for a gate density of 400k/mm^2 in 45-nm technology, translates to 0.24 mm^2. With a clock frequency of 70 MHz, the total power of the logic is estimated to be 10 mW.

Table I summarizes the measured performance and compares it with other state-of-the-art receivers. (Only [1] supports carrier aggregation.)

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References

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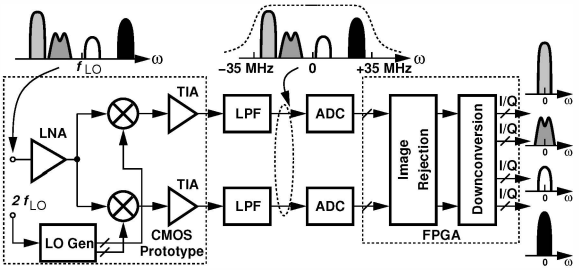

Fig. 1. Proposed receiver architecture.

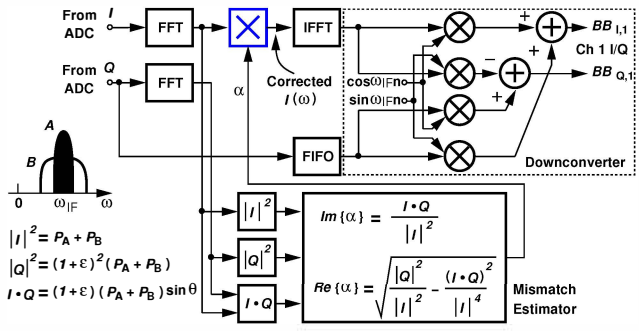

Fig. 2. Proposed image rejection and downconverter implementation.

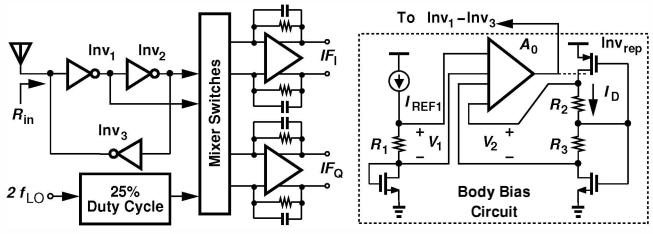

Fig. 3. Implementation of receiver front end.

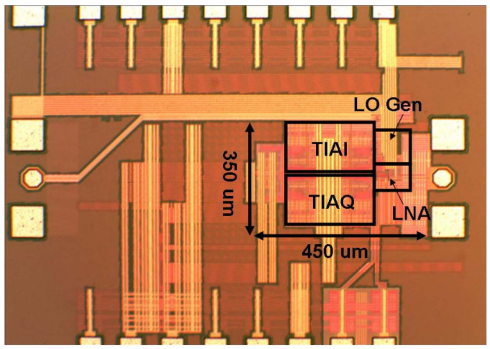

Fig. 4. Die photograph of receiver front end.

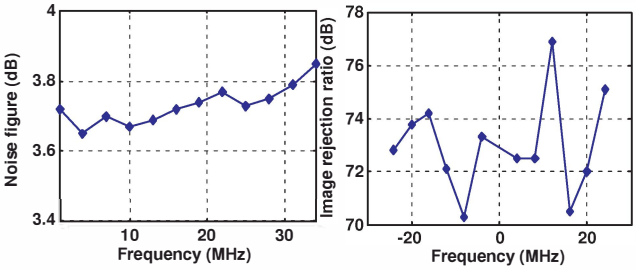

Fig. 5. Measured NF and image rejection ratio.

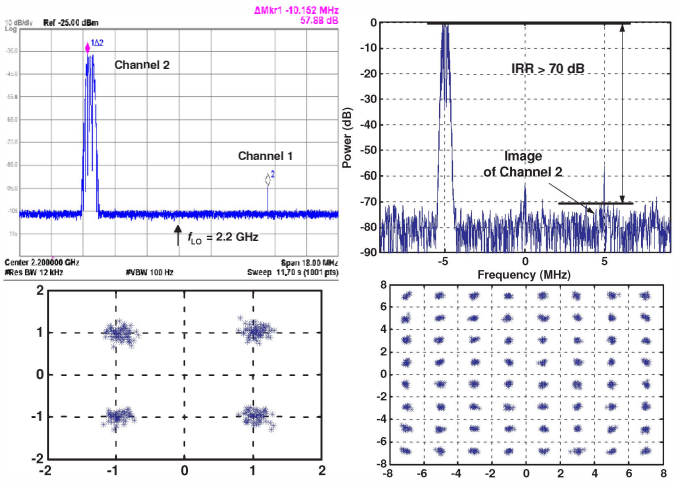

Fig. 6. Measured complex baseband spectrum and constellations.

TABLE1: Performance Summary

	This work	[1]	[6]	[7]
Standard	LTE	LTE	LTE	LTE/WCDMA
Architecture	Block Down.	Double Conv.	Direct Conv.	Direct Conv.
No. of Intra-Band Carriers	> 2	2	1	1
Tech. / Supply	45 nm / 1 V	65 nm / 1.45V	130 nm / 1.2V	90 nm / NA
Power	15 mW(1)	68 mW(2)	48 mW(3)	NA
IIP2 (duplex)	> 40 dBm	> 58 dBm	60 dBm	> 60 dBm
IIP3 (half-duplex)	2.75 dBm	2.4 dBm	-7 dBm	2 dBm
IIP2 (in-band)	31 dBm	27 dBm	NA	NA
IIP3 (in-band)	-13.7 dBm	-15 dBm	NA	-8 dBm
DSB NF	3.8 dB	4.5 dB	3.1 dB	3 dB
Voltage Gain	37 dB	45 dB	45 dB	60 dB
IRR	> 70 dB	> 55 dB	NA	NA

(1) LNA + Mixers + TIAs + LO gen.
(2) Estimated from ISSCC Visual Supplement for LNA + RF mixers + IF mixers, excluding the power of all IF and baseband filters.
(3) LNA + Mixers + TIAs + LO gen.