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Frequency-Based Measurement of Mismatches Between Small Capacitors[1]

Ashutosh Verma and Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles

Abstract

The mismatch between two capacitors can be measured by alternately switching each into an oscillator and measuring the change in the oscillation frequency. Three-stage differential ring oscillators can provide multiple mismatch data points for capacitances as small as 8 fF. Experimental results obtained from test circuits fabricated in 0.13-μm CMOS technology also reveal lower mismatches for metal sandwich capacitors than for lateral fringe structures.

I. Introduction

The need for measurement of mismatches between small capacitors arises in both process characterization and high-precision analog design. For example, multi-bit pipelined stages in analog-to-digital converters (ADCs) may incorporate a segmented digital-to-analog converter (DAC) having small unit capacitors whose matching determines the overall linearity. Similarly, charge-redistribution successive-approximation ADCs typically employ a capacitor DAC containing a large number of unit capacitors.

This paper introduces a capacitance-frequency conversion technique for the measurement of capacitor mismatches. Unlike voltage-based methods reported to date, the proposed approach provides the mismatch directly in digital form, simplifying the measurement and improving its reproducibility.

Section II of the paper describes design and measurement challenges in capacitor mismatch characterization. Section III presents the proposed method and identifies the sources of error that it entails. Section IV summarizes the experimental results.

II. Capacitor Mismatch Measurement Issues

Since direct measurement of small capacitors is prone to errors due to pad capacitance mismatches and the resolution of the instrumentation, on-chip circuitry is often necessary to isolate the devices under test from other parasitics. Figure 1 depicts an example, where the left plate of C_1 and the right plate of C_2 are switched between 0 and V_{REF} in opposite directions and the change at node E is measured [1]. This technique suffers from several drawbacks:

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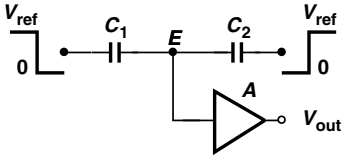

Fig. 1. Voltage-based mismatch measurement.

1. The input capacitance and noise of the buffer A corrupt the measurement.
2. The small change in V_E (fundamentally a single-ended quantity) is prone to noise in the setup and difficult to measure.
3. The unknown initial charge at node E may require a periodic reset mechanism, thus leading to kT/C noise.

Interestingly, while the kT/C noise due to the *total* sampling capacitance in an ADC is negligible, that due to *unit* capacitors in a segmented array may not be.

Figure 2 illustrates another example, where a ramp is applied to X while Y is grounded and vice versa [2, 3]. The

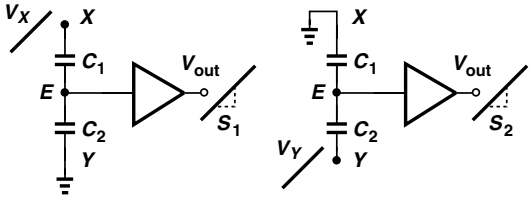

Fig. 2. Ramp-based mismatch measurement.

output voltage slopes, S_1 and S_2 are measured, and the difference between the slopes is translated to mismatch between C_1 and C_2:

$$\frac{C_1 - C_2}{C_1 + C_2} = \frac{S_1 - S_2}{S_1 + S_2}. \quad (1)$$

Owing to the "analog" nature of the measurement, this technique, too, suffers from inaccuracies due to the buffer and setup noise (and kT/C noise if E must be reset periodically). The above observations indicate a need for a capacitor mismatch characterization technique that does not rely on the measurement of voltages.

III. Proposed Technique

A. Basic Idea

Consider the conceptual arrangement shown in Fig. 3, where the oscillation frequency f_{out} is a function of C_1 or C_2. Thus,

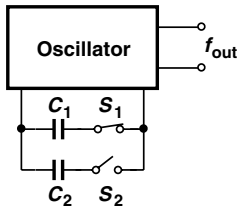

Fig. 3. Frequency-based mismatch measurement.

the relative mismatch between the capacitors, $\Delta C/C$, translates to a relative change in the frequency, $\Delta f_{out}/f_{out}$, if S_1 turns off and S_2 turns on. Since frequency quantities can be measured with much greater resolutions than voltage quantities, this approach potentially provides a high accuracy in capacitor mismatch characterization. For small mismatches, we can assume,

$$\frac{\Delta f_{out}}{f_{out}} = \alpha \frac{\Delta C}{C}. \tag{2}$$

Figure 4 depicts an embodiment of the above concept using a ring oscillator. In this topology, however, $\Delta f_{out}/f_{out}$

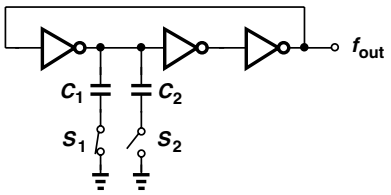

Fig. 4. Possible realization of the concept in Fig. 3.

is a strong function of the delays of the unloaded stages if C_1 and C_2 are small, making the relationship between $\Delta C/C$ and $\Delta f_{out}/f_{out}$ heavily process-dependent. (If C_1 and C_2 are so large that the unloaded stages contribute negligible delay, then the circuit may fail to oscillate.)

Figure 5 illustrates a modification that alleviates this dependence. In this uniformly-loaded ring, $\Delta f_{out}/f_{out}$ is about

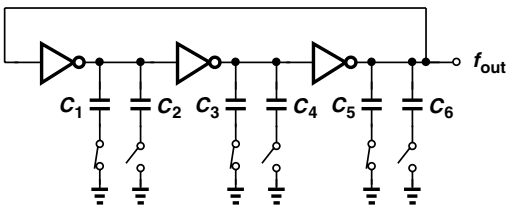

Fig. 5. Uniformly-loaded ring oscillator.

$(\Delta C/C)/3$ if C_1-C_6 are nominally equal. Furthermore, the structure provides three mismatch data points corresponding to the three pairs of capacitors, improving the efficiency of both layout and on-wafer measurements. Note that mismatches between the inverter delays slightly alter the value of α, but do not directly corrupt the capacitor mismatch results. For example, an inverter delay mismatch of 10% scales α by about 3.5%.

The high supply sensitivity of the inverters in Fig. 5 does present difficulties in on-wafer measurements. (In the first experimental prototype of this topology, the noise picked up by the probes and the dc drops along probe connections made it impossible to collect meaningful data.) The circuit is thus modified to the differential form shown in Fig. 6. While tol-

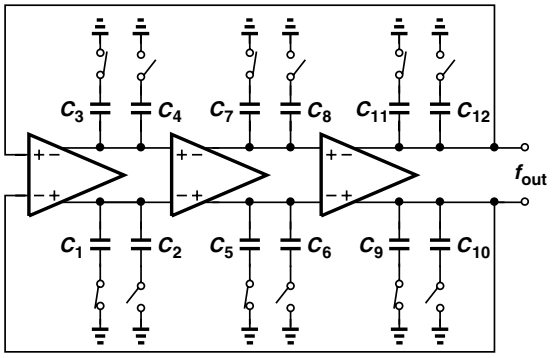

Fig. 6. Uniformly-loaded differential ring oscillator.

erating much greater common-mode noise, this implementation weakens the dependence of $\Delta f_{out}/f_{out}$ to approximately $(\Delta C/C)/6$. Each stage is realized as a simple differential pair with resistive loads. Note that the delays of such stages match more accurately than those of inverters, alleviating the dependence of α on stage delay mismatches.

B. Sources of Error

The proposed technique entails a few sources of error that impact the actual design of the test circuit and ultimately limit the precision with which the capacitor mismatch can be measured.

The first source of error relates to the mismatch between the on-resistances of S_1 and S_2 in Fig. 3 or their counterparts in Figs. 4, 5, and 6. If comparable with the driving resistance provided by the oscillator, the switch on-resistance, R_{on}, affects the oscillation frequency and, therefore, its mismatch becomes indistinguishable from capacitor mismatch. It is possible to increase the width of the switches to reduce their on-resistance and its mismatch, but the capacitance contributed by the switches creates other uncertainties (explained below). Alternatively, a large resistance can be placed in series with the output of each stage (Fig. 7) such that $R_T \gg R_{on1,2}$ (and $R_T \gg R_{on3,4}$), thus minimizing the effect of R_{on} on the frequency and making the mismatch between R_{on1} and R_{on2} (or R_{on3} and R_{on4}) a negligible contribution to $\Delta f_{out}/f_{out}$. Note that R_T can be almost arbitrarily large so long as its parasitic capacitance remains negligible, thereby overwhelming the mismatch between R_{on1} and R_{on2} (or R_{on3} and R_{on4}). Also, the mismatch between the two R_T's in Fig. 7 is unimportant.

The second source of error stems from the mismatch between the bottom-plate parasitics of the two capacitors under

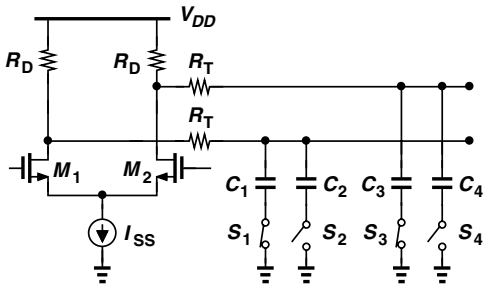

Fig. 7. Differential pair with series resistance.

test (Fig. 8)[2]. When S_1 is on and S_2 is off, the total capac-

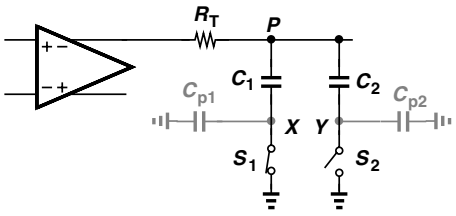

Fig. 8. Differential pair with parasitic capacitance.

itance at node P is equal to $C_1 + C_2C_{p2}/\left(C_2 + C_{p2}\right) \approx C_1 + C_{p2}$, because $C_{p2} \ll C_2$. After the switches change position, the capacitance becomes equal to $C_2 + C_{p1}$. Thus, the relative change in the delay of one stage is given by,

$$\begin{aligned} \frac{\Delta T_D}{T_D} &= \frac{C_2 + C_{p1} - (C_1 + C_{p2})}{C + C_p} \\ &= \frac{\Delta C + \Delta C_p}{C + C_p}, \end{aligned} \tag{3}$$

where C denotes the mean value of C_1 and C_2, and C_p the mean value of C_{p1} and C_{p2}. Fortunately, if, for example, $C_p/C \approx 5\%$, then it is likely that $\Delta C_p \ll \Delta C$. This is because the capacitors and their bottom-plate parasitics equally benefit from averaging over their respective areas and hence should exhibit roughly equal relative mismatches.

The input capacitance of the stages in the ring oscillator affects the value of α in $\Delta f_{out}/f_{out} = \alpha(\Delta C/C)$ to some extent, especially if it is comparable with the capacitance under test. Thus a calibration circuit is necessary to determine the value of α (Section IV).

The output buffer necessary to drive external instrumentation also introduces some imbalance among the three stages. For this reason, each stage is loaded with a replica of the output buffer.

IV. Experimental Results

In order to study the potential of the proposed technique, an extensive set of test circuits has been fabricated in 0.13-μm CMOS technology. Figure 9 shows the die photograph. The capacitor structures studied here are:

[2]The mismatch between the capacitances introduced by S_1 and S_2 at X and Y also translates to error, but with minimum-size devices, this component is negligible.

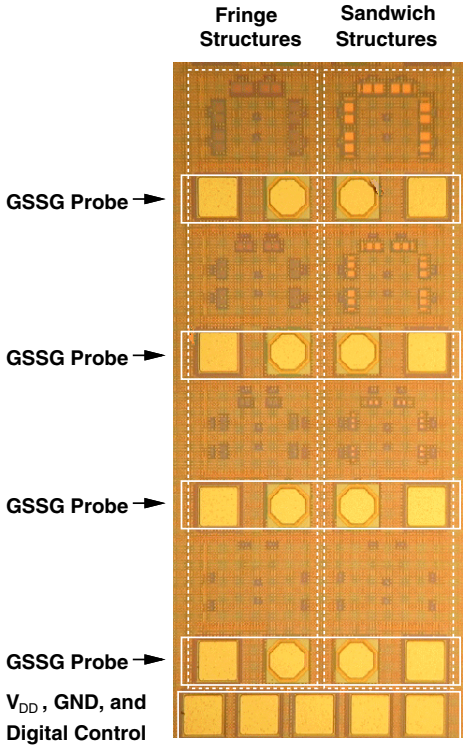

Fig. 9. Die photograph.

1. Metal 7 - metal 6 - metal 5 sandwich, 10 μm $\times$ 10 μm,
2. Metal 7 - metal 6 - metal 5 sandwich, 15 μm $\times$ 15 μm,
3. Lateral fringe structure (metal 6, metal 5, metal 4), 10 μm $\times$ 10 μm,
4. Lateral fringe structure (metal 6, metal 5, metal 4), 15 μm $\times$ 15 μm.

Each finger in structures 3 and 4 has a width of 0.20 μm. Six pairs of each capacitor are included in a three-stage differential ring oscillator (Fig. 6) so as to provide six mismatch data points.

All oscillators share the same digital select lines. As illustrated in Fig. 9, the oscillators are powered and controlled by a set of probes on the bottom. The frequencies are then measured through high-speed ground-signal-signal-ground (GSSG) probes, which are stepped vertically from one site to the next. Only one phase of the differential output is brought to a pad, allowing two oscillators to share one GSSG footprint.

As mentioned above, the capacitances contributed by the differential pairs appear as a constant term in the stage capacitance, thereby introducing some error in the value of α (which must be equal to $1/6$ in the ideal case). To eliminate this error, an unloaded differential ring oscillator (still including R_T and interconnect parasitics) serves as a calibration circuit.

The characterization proceeds as follows.

1. The oscillation frequency of the unloaded oscillator is measured on the wafer.
2. The value of R_T is adjusted in simulation to obtain the same unloaded oscillation frequency.

3. The oscillation frequency of a loaded oscillator is measured on the wafer.
4. The value of the capacitors is adjusted in simulations, so as to observe the same loaded oscillation frequency. This step also provides the nominal value of the capacitors under test, C_{nom}.
5. The loaded oscillator is simulated with a small capacitor mismatch to determine $\Delta f_{out}/f_{out} = \alpha(\Delta C/C)$ and hence the value of α.
6. With α known, the value of $\Delta f_{out}/f_{out}$ is measured on the wafer for each capacitor pair and translated to a value for $\Delta C/C$.

These steps are repeated for each of the four capacitor structures. The oscillation frequency is monitored by both a spectrum analyzer and a high-sensitivity frequency counter.

Figures 10-13 plot the measured distributions for 36 pairs of each capacitor structure. Noise picked up by the probes still limits the frequency resolution to about ±5 kHz (with loaded oscillation frequencies ranging from 57 MHz to 215 MHz). Nonetheless, the results shown in Figs. 10-13 provide an upper bound on the mismatches between the above capacitor structures. It is expected that the inclusion of a simple counter on the chip eliminates the effect of noise.

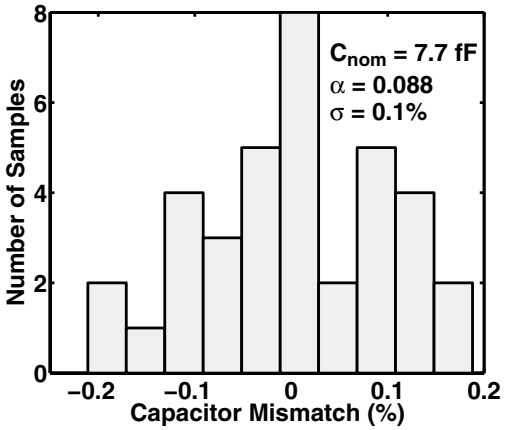

Fig. 10. Mismatch distribution for 10 μm × 10 μm sandwich structure.

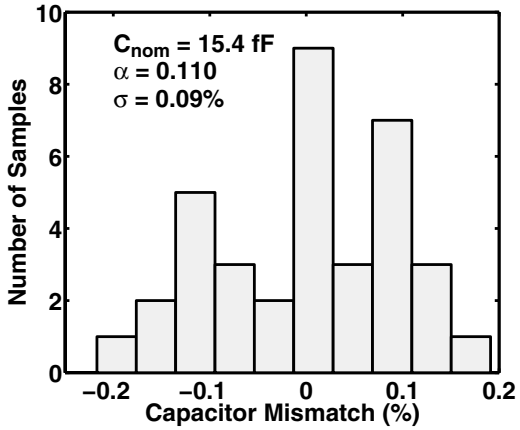

Fig. 11. Mismatch distribution for 15 μm × 15 μm sandwich structure.

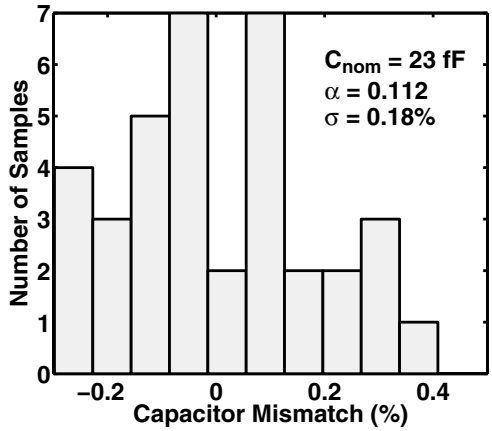

Fig. 12. Mismatch distribution for 10 μm × 10 μm lateral fringe structure.

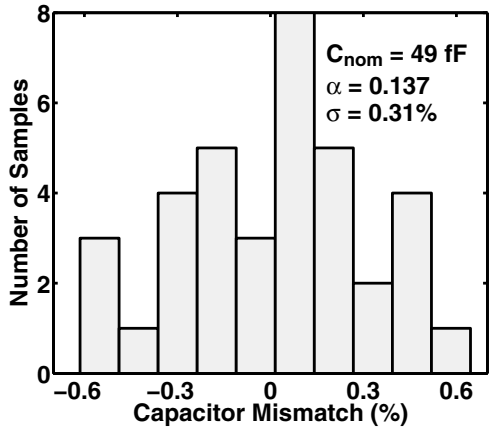

Fig. 13. Mismatch distribution for 15 μm × 15 μm lateral fringe structure.

The experimental distributions depicted in Figs. 10-13 indicate, for the first time, that lateral fringe capacitors exhibit greater mismatches than metal sandwich structures do. As expected, the narrow fingers provide a high lateral capacitance but suffer from substantial random variations in their width during fabrication.

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