A UWB CMOS Transceiver

Behzad Razavi, *Fellow, IEEE*, Turgut Aytur, Christopher Lam, *Member, IEEE*, Fei-Ran Yang, *Member, IEEE*, Kuang-Yu (Jason) Li, *Member, IEEE*, Ran-Hong (Ran) Yan, Han-Chang Kang, *Member, IEEE*, Cheng-Chung Hsu, and Chao-Cheng Lee

***Abstract*—A direct-conversion ultra-wideband (UWB) transceiver for Mode 1 OFDM applications employs three resonant networks and three phase-locked loops. Using a common-gate input stage, the receiver allows direct sharing of the antenna with the transmitter. Designed in 0.13-μm CMOS technology, the transceiver provides a total gain of 69–73 dB and a noise figure of 6.5–8.4 dB across three bands, and a TX 1-dB compression point of −10 dBm. The circuit consumes 105 mW from a 1.5-V supply.**

I. Introduction

ULTRA-WIDEBAND (UWB) communication by means of short "carrier-free" pulses was first conceived in "time-domain electromagnetics" in the 1960s [1], [2].[1] At the time, the low interceptibility and fine ranging resolution of UWB pulses made this type of signaling attractive to military and radar applications; but today, the potential for high data rates has ignited commercial interest in UWB systems. Both direct-sequence impulse communication and multiband orthogonal frequency division multiplexing (OFDM) are presently under consideration for the UWB standard.

This paper describes the design of the first UWB CMOS transceiver for Mode 1 multiband OFDM applications. Section II gives a system overview and Section III summarizes the receiver (RX) and transmitter (TX) specifications. Sections IV and V present the transceiver architecture and building blocks, respectively. Section VI deals with the experimental results.

II. System Overview

A. MBOA Standard

The Multiband OFDM Alliance (MBOA) standard for UWB communications draws heavily upon prior research in wireless local area network (WLAN) systems [3]. In a manner similar to IEEE 802.11a/g, MBOA partitions the spectrum from 3 to 10 GHz into 528-MHz bands and employs OFDM in each band to transmit data rates as high as 480 Mb/s. A significant departure from the original principle of "carrier-free" signaling, the multiband operation is chosen to both simplify the generation and detection of signals and leverage well-established OFDM solutions from WLAN systems. To ensure negligible interference with existing standards, the FCC has limited the output power level of UWB TXs to −41 dBm/MHz.

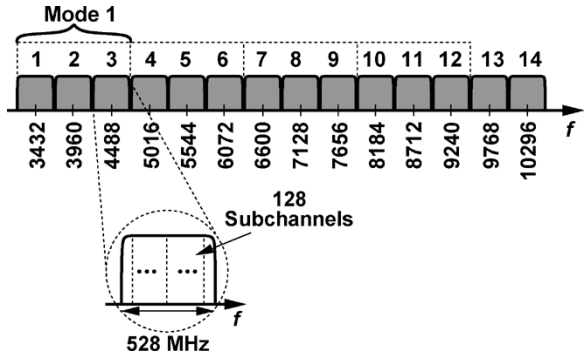


Fig. 1. MBOA band structure and channelization.

Fig. 1 shows the structure of the MBOA bands and the channelization within each band. The 14 bands span the range of 3168 to 10 560 MHz, with their center frequencies given by $m \times (264\ \text{MHz})$ for odd values of m from 13 to 39. Each band consists of 128 subchannels of 4.125 MHz. In contrast to IEEE 802.11a/g, MBOA employs only QPSK modulation in each subchannel to allow low resolution in the baseband analog-to-digital (A/D) and digital-to-analog (D/A) converters (4–5 bits). Bands 1–3 constitute "Mode 1" and are mandatory for operation, whereas the remaining bands are envisioned for high-end products.

In order to improve the robustness of the system with respect to multipath effects and interference, the standard complements OFDM with band hopping. In Mode 1, for example, the information bits are interleaved across all three bands and, as illustrated in Fig. 2, the system hops at the end of each OFDM symbol (every 312.5 ns). The band switching must occur in less than 9.47 ns, thereby posing difficult challenges in the design of the transceiver.

Table I compares the RX specifications of IEEE 802.11a and MBOA UWB systems for their respective maximum data rates.[2] The latter demands both a much more stringent noise figure (NF) and a much greater overall bandwidth in the RX and TX paths.

It is interesting to examine the NF requirements if MBOA had retained the IEEE 802.11a 64-QAM format. To raise the data rate from 54 to 480 Mb/s, the channel bandwidth B would need to increase from 20 to 178 MHz. Writing

$$\text{Sensitivity} = -174\ \text{dBm} + 10\log B + \text{NF} + \text{SNR} \qquad (1)$$

Manuscript received April 26, 2005; revised July 15, 2005.

B. Razavi is with the Electrical Engineering Department, University of California, Los Angeles, CA 90095-1594 USA (e-mail: razavi@ee.ucla.edu).

T. Aytur, C. Lam, F.-R. Yang, K.-Y. Li, and R.-H. Yan are with Realtek Semiconductor, Irvine, CA 92618 USA.

H.-C. Kang, C.-C. Hsu, and C.-C. Lee are with Realtek Semiconductor, Hsinchu, Taiwan, R.O.C.

Digital Object Identifier 10.1109/JSSC.2005.857430

[1]The term "ultra-wideband" was evidently coined by the U.S. Department of Defense in the 1980s.

[2]The MBOA modulation for maximum bit rate has recently changed to "dual-carrier modulation" (DCM) but the required SNR remains the same.

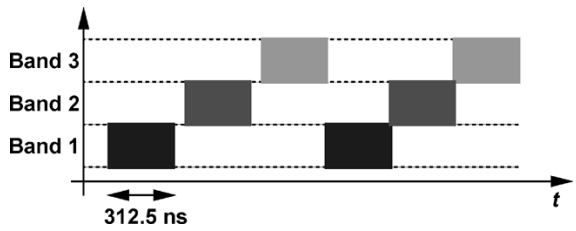


Fig. 2. Band hopping in MBOA.

TABLE I
COMPARISON OF IEEE 802.11A AND MBOA SPECIFICATIONS

	IEEE 802.11a	MBOA UWB
Sensitivity	−65 dBm	−73 dBm
Data Rate	54 Mb/s	480 Mb/s
Channel BW	20 MHz	528 MHz
Modulation	64−QAM	QPSK
SNR (BER =10^{-5})	23 dB	8 dB
RX NF	12−14 dB	6−7 dB

where SNR denotes the required signal-to-noise ratio, and assuming SNR $=$ 23 dB for a bit error rate (BER) of 10^{-5}, we have

$$\text{Sensitivity} = -68.5\ \text{dBm} + \text{NF}. \tag{2}$$

That is, it would have been impossible to achieve a sensitivity of -73 dBm. On the other hand, if SNR is relaxed by reducing the order of the modulation, the sensitivity can be improved even though $10 \log B$ increases to some extent. In particular, with SNR $= 8$ dB for QPSK modulation and $B = 528$ MHz

$$\text{Sensitivity} = -79\ \text{dBm} + \text{NF} \tag{3}$$

indicating that an NF of about 6 dB yields the required sensitivity.[3]

One can attribute the foregoing significant improvement in sensitivity to Shannon's theorem:

$$C = B \log_2(1 + \text{SNR}) \tag{4}$$

where C denotes the capacity. Since C exhibits a stronger dependence on B than on SNR, higher data rates are more efficiently afforded by raising the symbol rate (with low-order modulation) than by requiring a high-order modulation (with low symbol rate).

B. Problem of Band Hopping

As mentioned above, the MBOA standard exploits frequency diversity through band hopping while demanding a settling time of only 9.47 ns. Since typical phase-locked loops (PLLs) take several hundred input cycles to settle, it is not possible to accommodate such fast band switching in a phase-locked synthesizer. This issue dominates the choice of frequency planning.

Another difficulty arising from band hopping relates to offset cancellation in the baseband. On one hand, DC offsets change in different bands and, on the other hand, analog offset cancellation circuits cannot settle in 9.47 ns if they must not attenuate the lowest OFDM subchannels (a few megahertz away from zero). For this reason, (coarse) offset cancellation can be performed by measuring and digitally storing the offsets for each band during the preamble and applying the results through D/A converters during payload.

[3]Owing to the coding gain in the system, the NF can be a few decibels higher.

C. Frequency Synthesis by Single-Sideband Mixing

In order to generate "agile" local oscillator (LO) signals, two frequencies can be added or subtracted by means of single-sideband (SSB) mixers [5]. However, SSB mixing, particularly in CMOS technology, presents a number of difficult spur issues. First, at least one port of each "submixer" must be linear to avoid mixing harmonics of that input with those of the other. The required linearization translates to a low conversion gain, small output swings, and hence the need for power-hungry (and perhaps inductor-hungry) buffers. Second, the waveforms applied to the linear ports must themselves exhibit low distortion, a difficult problem at gigahertz frequencies. Third, phase and gain mismatches in quadrature paths and within the mixers introduce additional spurs. Fourth, DC offsets lead to leakage of the input components to the output. Of particular concern here are spurious components that fall in the IEEE 802.11a/g bands as they can corrupt the down-converted signal in the presence of large WLAN interferers.

III. TRANSCEIVER SPECIFICATIONS

The design of UWB transceivers faces the following issues: 1) the need for broadband circuits and matching; 2) gain switch in the low-noise amplifier (LNA) without degrading the input match; 3) broadband transmit/receive switch at the antenna; 4) desensitization due to WLAN interferers; and 5) fast band hopping.

With a 528-MHz channel bandwidth, the RX and TX paths of UWB systems may naturally employ direct conversion. Typical direct-conversion issues plague the receive path, except that flicker noise negligibly affects the signal. Also, the TX side is free from injection pulling of the oscillator by the output stage because the transmitted level falls below -41 dBm/Hz. (The wide PLL bandwidth also suppresses the pulling [4].) This section describes the transceiver specifications, derived from the MBOA requirements and extensive system simulations.

Particularly important here is the maximum tolerable synthesizer phase noise as it determines the choice between ring and LC oscillators. In order to quantify the effect on the constellation, system-level simulations are performed wherein a QPSK-modulated OFDM signal carrying a data rate of 480 Mb/s is subjected to phase noise and the resulting BER is measured. Fig. 3(a) shows the phase noise profile assumed in simulations and Fig. 3(b) plots the BER as a function of the SNR for various profiles. Each profile is characterized with a "plateau" level $S_{\phi 0}$ and a corner frequency f_c. Since the rotation of the signal constellation is given by the total integrated phase noise, the degradation depends on both the magnitude of the plateau and the corner frequency. It is observed that a plateau phase noise of

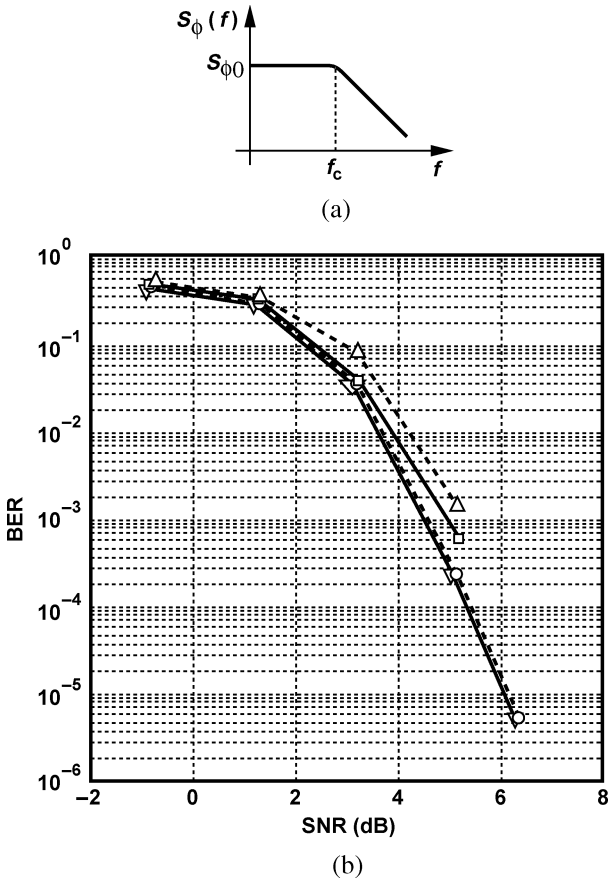


Fig. 3. (a) Phase noise profile assumed in system simulations. (b) Effect of phase noise on BER ($\triangledown : S_{\phi 0} = 0$; $\circ : S_{\phi 0} = -100$ dBc/Hz, $f_c = 5$ MHz; $\square : S_{\phi 0} = -87$ dBc/Hz, $f_c = 924$ kHz; $\triangle : S_{\phi 0} = -70$ dBc/Hz, $f_c = 924$ kHz).

-100 dBc/Hz with $f_c \approx 5$ MHz affects the performance negligibly, making ring oscillators (along with wideband synthesizers) a viable solution.

A. Receiver

Depending on the bit rate, MBOA specifies RX sensitivities ranging from -84 dBm (for 55 Mb/s) to -73 dBm (for 480 Mb/s). With a required SNR of about 8 dB, these specifications translate to an NF of 6–7 dB. The RX must provide a maximum voltage gain of approximately 84 dB so as to raise the minimum signal level to the full scale of the baseband A/D converter. Also, based on the interference expected from IEEE 802.11a/g transmitters, a 1-dB compression point $(P_{1\mathrm{dB}})$ of -23 dBm (in the high-gain mode) is necessary.

Table II summarizes the required performance. The phase noise specification is tightened by 5 dB with respect to the value obtained above to allow similar corruption in the TX. Note that the LNA must accommodate a gain switch of 16–20 dB to avoid excessive nonlinearity (due to the mixer and subsequent stages) in the OFDM signal as the received level exceeds -40 dBm. The total range for automatic gain control (AGC) is 60 dB.

The baseband channel-select filter must be designed in conjunction with the A/D converter. Greater stopband rejection provided by the former relaxes the sampling rate of the latter. For example, a third-order Butterworth response necessitates a sampling rate of about $4 \times 264 = 1056$ MHz. The A/D converter resolution is determined by the tolerable quantization noise, the AGC resolution, and the level of WLAN interferers that are only partially attenuated by the filter.

TABLE II
REQUIRED RX PERFORMANCE

Sensitivity	–84 to –73 dBm
NF	6–7 dB
$P_{1\,dB}$	–23 dBm
I/Q Mismatch	6° and 0.6 dB
Phase Noise	–105 dBc/Hz (Plateau)
Voltage Gain	84 dB
LNA Gain Switch	16–20 dB
Total AGC Range	60 dB
ADC	5–Bit, 528–1056 MHz

TABLE III
REQUIRED TX PERFORMANCE

DAC	5–Bit, 528–1056 MHz
I/Q Mismatch	6° and 0.6 dB
Output Power	–10 dBm
Output $P_{1\,dB}$	–6 dBm
Carrier Leakage	–30 dBc
Phase Noise	–105 dBc/Hz (Plateau)

B. Transmitter

The TX performance follows corresponding observations in the RX and is summarized in Table III. The maximum carrier leakage is chosen so that the TX incurs negligible degradation in the error vector magnitude (EVM). Note that, despite the large peak-to-average ratio of OFDM signals, the TX can operate with only a 4-dB backoff from the 1-dB compression point. This is because the large peaks appear infrequently and, more importantly, QPSK signals degrade very gradually by the intermodulation of OFDM subchannels when compression occurs. (By contrast, 64-QAM modulation typically requires an additional 5 dB of backoff for proper operation.)

IV. TRANSCEIVER ARCHITECTURE

Fig. 4 shows the transceiver architecture. (The circuitry in the dashed box contains quadrature components but is drawn with only one phase for clarity.) The receive path consists of an LNA having three resonant loads corresponding to the three bands, with each load driving selectable quadrature mixers. The down-converted signal is applied to a fourth-order Sallen-and-Key (SK) filter and a first-order low-pass stage. This amount of filtering allows ADC sampling rates slightly greater than 512 MHz. An AGC range of 60 dB is distributed as 16 dB in the LNA, 30 dB at the output of the mixers, and 14 dB in the baseband. The transmit path similarly employs fourth-order SK filters, up-conversion mixers, and an output stage that shares the antenna with the LNA.

The LO frequencies are synthesized using three independent PLLs to avoid SSB mixing. Running with a reference frequency of 66 MHz, each PLL generates quadrature phases and con-

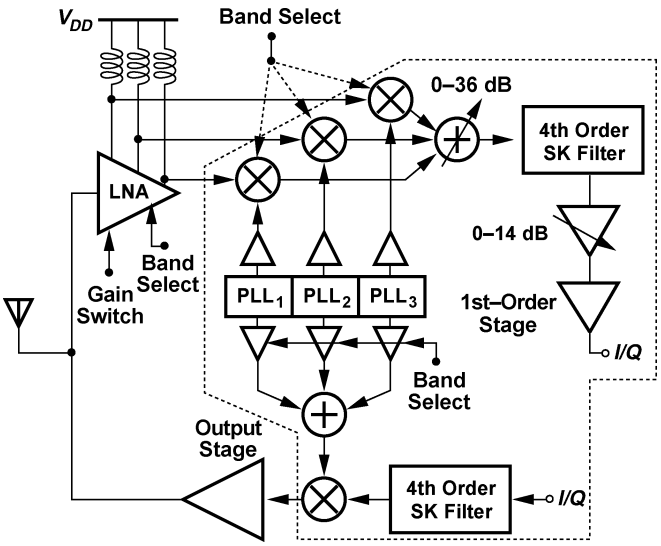


Fig. 4. Transceiver architecture.

sumes 15 mW, less than the power required by two sets of SSB mixers that would produce comparable output swings.

Three aspects of the above approach to frequency synthesis should be noted. First, the use of a 66-MHz reference allows a loop bandwidth of about 5 MHz, thus suppressing the close-in phase noise of the oscillators considerably. Second, the reference spurs at $n \times 66$ MHz offset fall within the desired channel for $n \leq 4$; i.e., only spurs resulting from the fifth and higher order harmonics of the reference must be sufficiently small, a point that eases the tradeoff between the loop bandwidth and the spur levels in the design of PLLs. Third, since the three PLL frequencies are far from each other and not related by integer multiples, injection pulling is negligible.

V. Building Blocks

A. Low-Noise Amplifier

In order to achieve both a broadband input match and a broadband transfer, inductively degenerated CMOS cascode LNAs can incorporate 1) an additional input bandpass network that cancels the reactive part of the input impedance across a wide frequency range [6], and 2) an inductively peaked resistive load to broaden the output bandwidth [6]. The principal issue here is that the inductors used in the input network introduce loss, raising the NF. Moreover, with a 1.2-V supply, it becomes increasingly difficult to accommodate a large DC drop across the load resistor and hence obtain a reasonable gain.

Fig. 5 shows the LNA topology used in this paper. A common-gate stage provides an input resistance of 50 Ω and the large (20 nH) inductor L_1 resonates with the total capacitance at the input at about 4 GHz, thereby yielding adequate return loss across the Mode 1 frequency range without degrading the NF. The required 16-dB gain switch is realized by turning M_1 off ($W_2 = W_1/8$), and the resulting increase in input resistance is compensated by turning M_6 on. The on-resistance of M_6 varies with process and temperature, but the correction still guarantees $S_{11} > 10$ dB under all conditions.

Transistors M_3–M_5 serve as switched cascode devices with tanks resonating at the center frequency of each band. The Q of the tanks is reduced to about 3 by addition of a parallel resistance to ensure a small droop near the band edges. With no series resistance necessary in the loads, the circuit can achieve a high gain at low supply voltages. Each output drives a set of quadrature mixers.

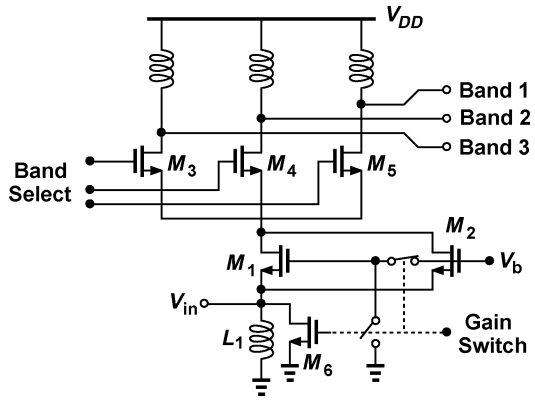


Fig. 5. LNA circuit.

Simulations indicate that the LNA displays an NF of 3.3 dB and a voltage gain of 22 dB while drawing 2.5 mA from the supply.

B. Mixer

Fig. 6 depicts the down-conversion mixer circuit. The single-balanced topology incorporates resistor R_H to halve the bias current commutated by M_2 and M_3, thereby allowing these transistors to switch more abruptly and hence inject less noise to the output. Furthermore, for a given voltage headroom, the mixer load resistance can be doubled, raising the conversion gain by 6 dB.

In order to ensure accurate current splitting between R_H and the switching pair, the common-mode level of the LO port is defined by means of a tracking circuit. As illustrated in Fig. 6, with M_5 carrying $I_2 = 0.25I_B$, a current of $0.25I_B$ must flow through $2R_H$, yielding $V_X = V_{\rm DD} - 0.5R_HI_B$ and thus $V_Y = V_{\rm DD} - 0.5R_HI_B + V_{\rm GS5}$. Consequently, $V_P = V_{\rm DD} - 0.5R_HI_B + V_{\rm GS5} - V_{\rm GS2,3}$, reducing to $V_{\rm DD} - 0.5R_HI_B$ if $V_{\rm GS5} \approx V_{\rm GS2,3}$ and, therefore, establishing a current of $0.5I_B$ through R_H.

The mixer must provide 30 dB of gain variation in steps of 6 dB. To this end, each load resistor is decomposed into six binary-weighted segments and the output current of the mixer is routed to one of the nodes according to the gain setting. The six PMOS switches required here must be wide enough to consume minimal voltage headroom while allowing a bandwidth of greater than 300 MHz at the output.

In addition to high linearity, the gain switching scheme in Fig. 6 also provides a constant output impedance. This property proves essential to the design of the subsequent baseband filter.

Simulations predict an NF of 16 dB and a voltage conversion gain of 10 dB for the mixer with a supply current of 2.5 mA.

C. Baseband Filter

With a mixer gain of 10 dB, the LNA/mixer cascade tends to experience compression at the output of the mixer. To alleviate this issue, the baseband filter can create a low impedance at the

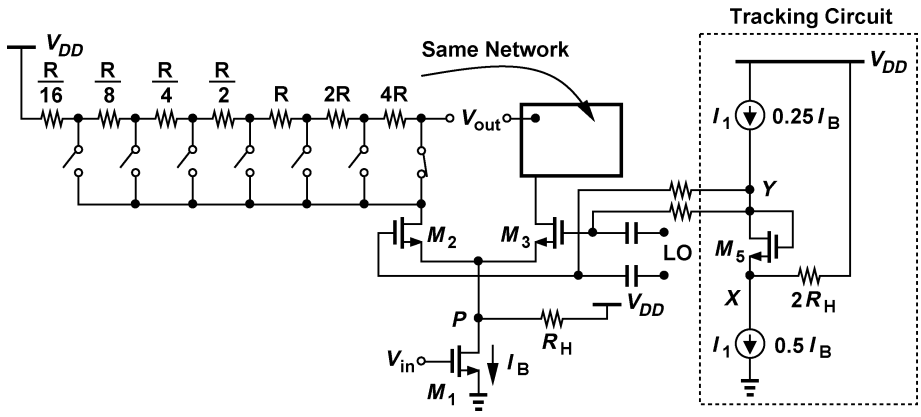


Fig. 6. Mixer circuit.

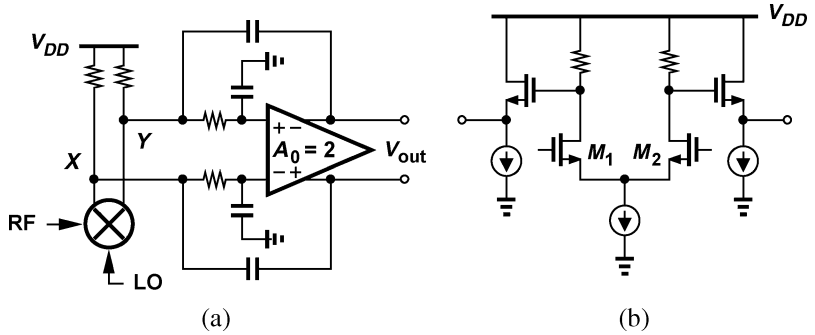


Fig. 7. (a) SK filter topology and its interface with mixer. (b) Core amplifier circuit.

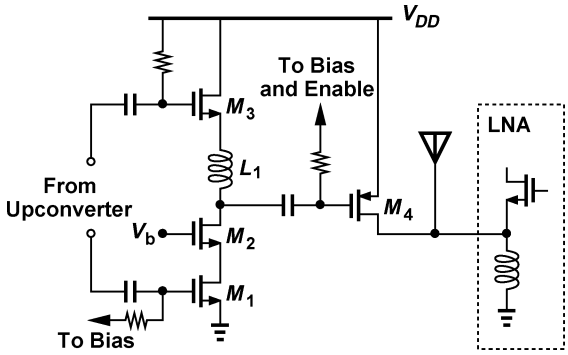


Fig. 8. TX diagram.

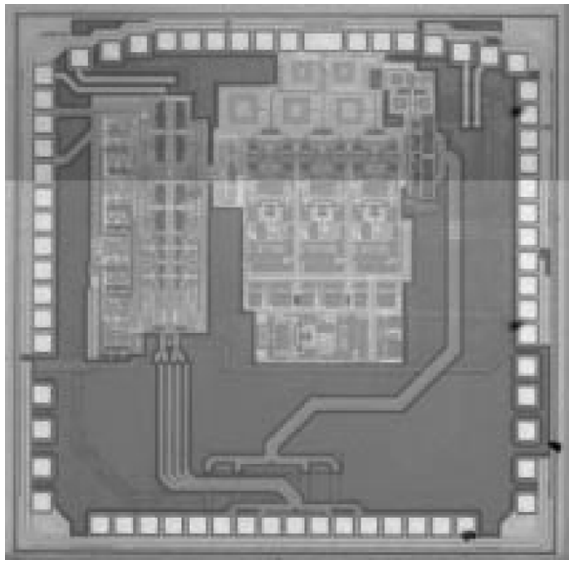


Fig. 9. Die photograph.

mixer output (at the interferer frequency) and hence reduce the voltage swing at these nodes considerably.

Fig. 7(a) shows the SK filter design and its interface with the mixer. The (binary-weighted) load resistors of the mixer serve as part of the filter, and the core amplifier employs a gain of 2. Despite the low open-loop gain, the filter lowers the interferer voltage swings[4] at nodes X and Y by about 3 dB, moving the compression bottleneck to the input of the mixer.

Fig. 7(b) shows the core amplifier. To obtain an open-loop bandwidth of greater than 1 GHz, the circuit incorporates a simple linearized differential pair and source followers.

D. TX Front End

Unlike the RX, the TX must accommodate the Mode 1 frequency range in only a single signal path to avoid complicating the interface with the antenna. The TX comprises double-balanced quadrature up-conversion mixers followed by the front end shown in Fig. 8. The differential signal produced by the mixers is applied to the differential to single-ended (D/S) converter consisting of M_1–M_3 and L_1. Here, L_1 serves as a shunt peaking element for the cascode and as a series peaking element for the source follower. Owing to the finite output impedance of the follower and hence nonideal series peaking, the D/S conversion does not double the signal swing but still helps to reduce the size of the output transistor M_4.

[4]The worst-case interferer lies above the third band, namely, at 5.15 GHz, and is down-converted to 670 MHz along with the desired signal.

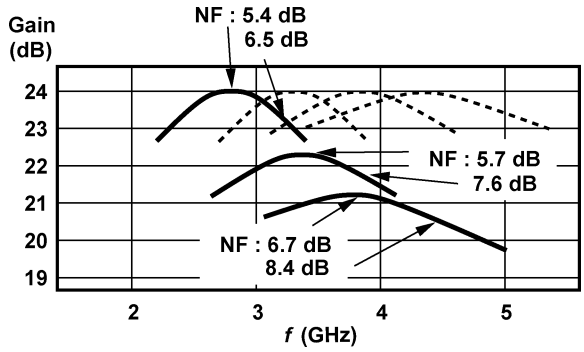


Fig. 10. Measured gain and NF.

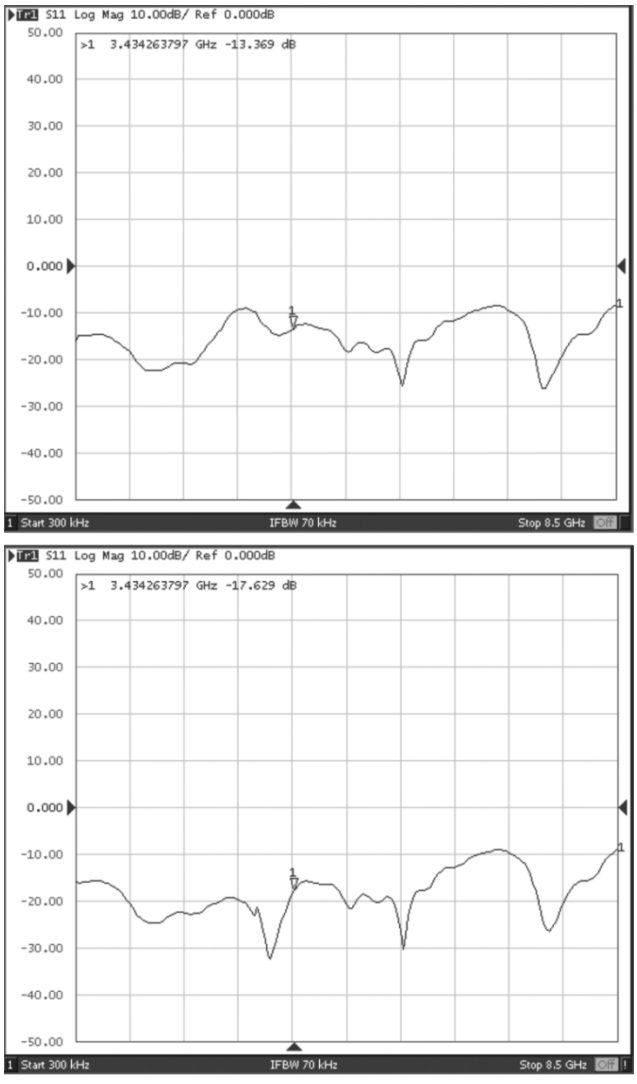


Fig. 11. Measured return loss for high gain (top) and low gain (bottom).

To avoid a transmit/receive switch, this design directly shares the antenna between the TX output stage and the LNA. The choice of W_4 and hence the capacitance that it introduces at the output entails a tradeoff between the TX output level and the degradation in the RX NF. Designed for an output power of -10 dBm, M_4 raises the NF by 0.15 dB.

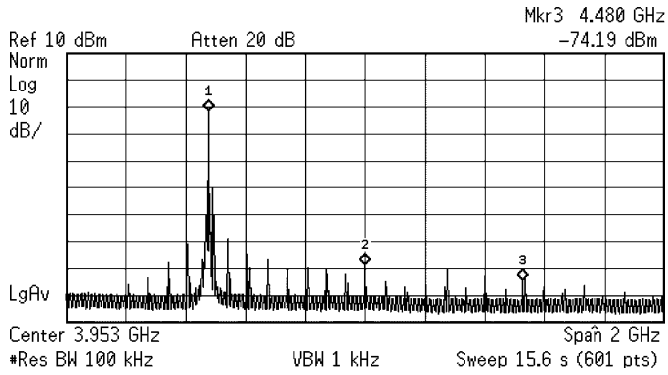


Fig. 12. Output spectrum of one PLL with the other two off.

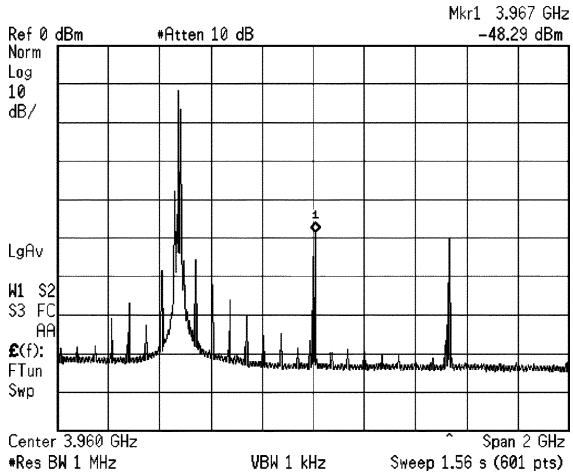


Fig. 13. Output spectrum of one PLL with the other two on.

VI. Experimental Results

The transceiver has been fabricated in 0.13-μm digital CMOS technology. Fig. 9 shows a photograph of the die, whose active area measures approximately 1 mm $\times$ 1 mm. The circuit is tested with a 1.5-V supply.

Fig. 10 plots the measured frequency response of the LNA across the three bands with the corresponding NFs shown on each plot. Due to inductor modeling inaccuracies, the center frequencies are shifted down and the gain is reduced in the upper bands. (The dashed plots indicate the desired characteristics.) These deviations can be corrected by adjusting the design of the inductors in subsequent silicon iterations.

Fig. 11 plots the input return loss for high and low LNA gains. The magnitude of S_{11} remains above 11 dB across the three bands in both cases.

Depicted in Fig. 12 is the output spectrum of one PLL while the other two are off. It is observed that the reference sidebands fall well below 60 dBc as they approach the WLAN bands. The same holds for the other two PLLs.

Fig. 13 shows the output spectrum of one PLL while the other two are on. The coupling of the oscillators through the supplies results in a relatively high level of spurs at the center frequencies of the other two bands, thereby lowering the tolerance of the RX to interference produced by the other UWB devices (but not

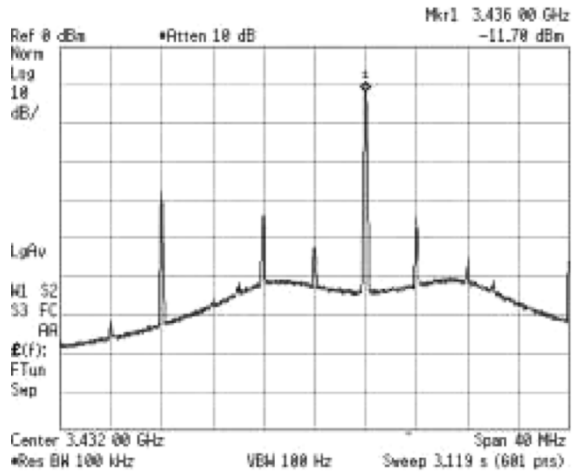


Fig. 14. TX output.

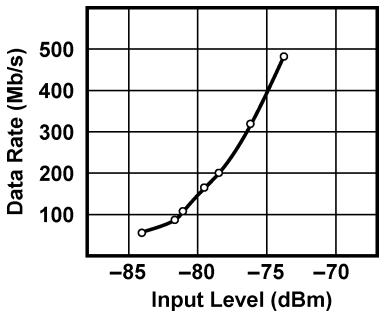


Fig. 15. Measured data rate as a function of input level.

TABLE IV
MEASURED TRANSCEIVER PERFORMANCE

Voltage Gain	**69–73 dB**
Noise Figure	**6.5 – 8.4 dB**
In–Band 1–dB Compression Point	
High LNA Gain	**–27.5 – –29.5 dBm**
Low LNA Gain	**–9.5 – –12.5 dBm**
S11	
High LNA Gain	**–12 dB**
Low LNA Gain	**–11 dB**
TX Output 1–dB Comp.	**–10 dBm**
Phase Noise @ 1–MHz Offset	**–104 – –106 dBc/Hz**
Power Dissipation	**105 mW**
Supply Voltage	**1.5 V**
Technology	**0.13–um CMOS**

WLAN TXs). On-chip filtering of the supplies is expected to suppress this coupling.

Shown in Fig. 14 is the close-in output spectrum of the TX in response to sinusoidal baseband signals, indicating an output level of -11.7 dBm (including a cable loss of 1 dB) and a plateau phase noise of approximately -104 dBc/Hz. The sidebands arise from carrier leakage and I/Q mismatch, but their level appears to be adequately low for QPSK modulation.

Fig. 15 plots as a function of the input level the data rate that the second channel of the RX can detect with BER $= 10^{-3}$. In this test, a Tektronix arbitrary waveform generator (AWG520) provides quadrature baseband OFDM signals to a discrete up-converter whose output is used to drive the UWB RX. The RX quadrature outputs are sampled by high-speed Gage digitizers and fed to a Matlab program, and the result is compared with the data produced by AWG520 to determine the BER.

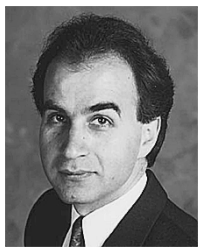
Table IV summarizes the transceiver performance. The range of values for the voltage gain, NF, $P_{1\mathrm{dB}}$, and phase noise corresponds to different bands. The TX output compression point is 4 dB lower than required and can be raised by increasing the bias current of the output stage.

ACKNOWLEDGMENT

The authors wish to thank J. Li, B. Lin, J. Chen, Y.-S.-K. Hsien, J. Spaven, J. Rollins, J. Yi, L. Tien, X. Fan, and S. Chen for their contributions to this paper.

REFERENCES

[1] G. F. Ross, "The transient analysis of certain TEM mode four-port networks," *IEEE Trans. Microw. Theory Tech.*, vol. MTT-14, no. 11, pp. 528–547, Nov. 1966.
[2] C. L. Bennet and G. F. Ross, "Time-domain electromagnetics and its applications," *Proc. IEEE*, vol. 66, no. 3, pp. 299–318, Mar. 1978.
[3] *Multi-Band OFDM Physical Layer Proposal, IEEE 802.15-03/268r5*, Nov. 2003.
[4] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.
[5] D. Leenaerts *et al.*, "A SiGe BiCMOS 1-ns fast hopping frequency synthesizer for UWB radio," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2005, pp. 202–203.
[6] A. Bevilacqua and A. Niknejad, "An ultrawideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2004, pp. 382–383.



Behzad Razavi (S'87–M'90–SM'00–F'03) received the B.S.E.E. degree from Sharif University of Technology, Tehran, Iran, in 1985, and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, in 1988 and 1992, respectively.

He was an Adjunct Professor with Princeton University, Princeton, NJ, from 1992 to 1994, and at Stanford University in 1995. He was with AT&T Bell Laboratories and Hewlett-Packard Laboratories until 1996. Since 1996, he has been an Associate Professor and, subsequently, a Professor of electrical engineering with the University of California, Los Angeles. He is the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice-Hall, 1998) (translated into Chinese and Japanese), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001) (translated into Chinese and Japanese), and *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003), and the editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996) and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003). His current research includes wireless transceivers, frequency synthesizers, phase-locking and clock recovery for high-speed data communications, and data converters. He has served as an Associate Editor for the *International Journal of High Speed Electronics*.

Prof. Razavi is an IEEE Distinguished Lecturer. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS. He was the recipient of the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, and the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC. He was also recognized as one of the top ten authors in the 50-year history of ISSCC.

Turgut Aytur received the B.S.E.E. degree from Princeton University, Princeton, NJ, in 1993, the M.S.E.E. degree from Columbia University, New York, NY, in 1996, and is currently working toward the Ph.D. degree in electrical engineering at the University of California, Berkeley, where he has worked on the development of CMOS sensors for biological applications.

From 1993 to 2003, he was with AT&T Bell Laboratories/Lucent Technologies, Holmdel, NJ, where he worked on analog integrated circuits for cellular and wireless local area network applications. Since 2003, he has been with Realtek Semiconductor, Irvine, CA, where he is a Product Director for wireless communications.

Christopher Lam (M'03), photograph and biography not available at the time of publication.

Fei-Ran Yang (S'97–M'01) received the B.S. degree in communication engineering from the National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 1993, the M.S. degree from the University of Michigan, Ann Arbor, in 1996, and the Ph.D. degree in electrical engineering at the University of California, Los Angeles, in 2000, respectively.

From 2000 to 2001, he was with Malibu Networks, Calabasas, CA, designing the upper U-NII band RF transceivers for fixed wireless broadband access. He joined Orion Microelectronics, Irvine, CA, a subsidiary of Realtek Semiconductor, in 2002, as an RF System Engineer engaged in the development of dual-band wireless local area network transceivers and ultrawideband transceivers.

Kuang-Yu (Jason) Li (M'03) was born in Taiwan, R.O.C., in 1965. He received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1987, and the M.S. and Ph.D. degrees from the University of Southern California, Los Angeles, in 1991 and 1995, respectively.

From 1995 to 2000, he was with Hughes Space and Communications Company, designing and developing a geostationary mobile satellite communications system, where he was responsible for system architecture and requirements definition, analysis, and simulation. In 2000, he was with Malibu Networks, where he contributed to an OFDM modem design and system analysis on adaptive modulation, power control, interference analysis, and cell planning for fixed broadband wireless applications. Since 2002, he joined Orion Microelectronics, a Realtek group, Irvine, CA, as an RF Systems Director. He leads a system team in the design, verifications, integration, and production of wireless local area network and ultrawideband wireless systems.

Ran-Hong (Ran) Yan received B.S.E.E. degree from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1984, and the M.S. and Ph.D. degrees from the University of California, Santa Barbara, in 1987 and 1990, respectively.

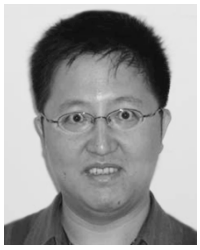
He then joined Bell Labs Research, working on deep-submicron CMOS technology and low-power electronics. While at Bell Labs, he became a Department Head for Microsystems Research in 1995, where he was responsible for circuit design issues on advanced silicon technology, bipolar CMOS, and SiGe research. He then took on the responsibility for the High Speed Circuits and Systems Research Department in 1996, and as the Director of Global Wireless Systems Research Department in 1997. He was named Vice President of Wireless Research Lab in 2001, supporting Lucent's Mobility business with leading edge research at the physical and media-access control layers. He joined Realtek Semiconductor, Irvine, CA, in 2003 as a Senior Vice President for Wireless Communications, responsible for wireless local area network, personal area network, and RF for multimedia solutions.

Han-Chang Kang (A'04–M'04) received the B.S. and M.S. degrees in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, R.O.C., in 2000 and 2002, respectively.

He joined Realtek Semiconductor, Hsinchu, in 2003, where he is an RF Circuit Designer in the RF Group. His primary interest is in RF front-end circuits with current focus on RF frequency synthesizers and voltage-controlled oscillators.

Cheng-Chung Hsu was born in Chang-Hua, Taiwan, R.O.C., in 1975. He received the B.S. and Ph.D. degrees in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan, in 1997 and 2003, respectively.

He is currently a Senior Engineer with Realtek Semiconductor, Hsinchu. His research interests include analog front-end circuits in data communication.



Chao-Cheng Lee received the B.S. degree in electrical engineering from the National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1988, and the M.S. degree in physics from the National Taiwan University, Taipei, Taiwan, in 1990.

He joined Realtek Semiconductor, Hsinchu, in 1992 and is currently the Director of the Research and Development Center. His research interests includes phase-locked loops, filters, and high-speed circuits. He has more than 20 U.S. patents granted or pending.